

AM64x/AM243x GENERAL PURPOSE EVM BOARD

PROC101B

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REV	B
VER	1.0

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Size
C Variant Name = PROC101B(001) TMDSE44GPEVM

Rev
E2

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REVISION HISTORY

VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
0.1	26th MAY 2021	Drafted from "PROC101A_SCH" document.	Mistral Design Team	AJIT MB	AJIT MB
0.2	3rd JUNE 2021	Added Voltage Monitor on 0.85V for ensuring required power down sequence is followed	Mistral Design Team	AJIT MB	AJIT MB
0.3	9th JUNE 2021	Changed Clock Generator VDDO level to 1.8V	Mistral Design Team	AJIT MB	AJIT MB
0.4	1st DEC 2021	Updated LM5140 Section	Mistral Design Team	AJIT MB	AJIT MB
1.0	3rd DEC 2021	Baselined and Released	Mistral Design Team	AJIT MB	AJIT MB

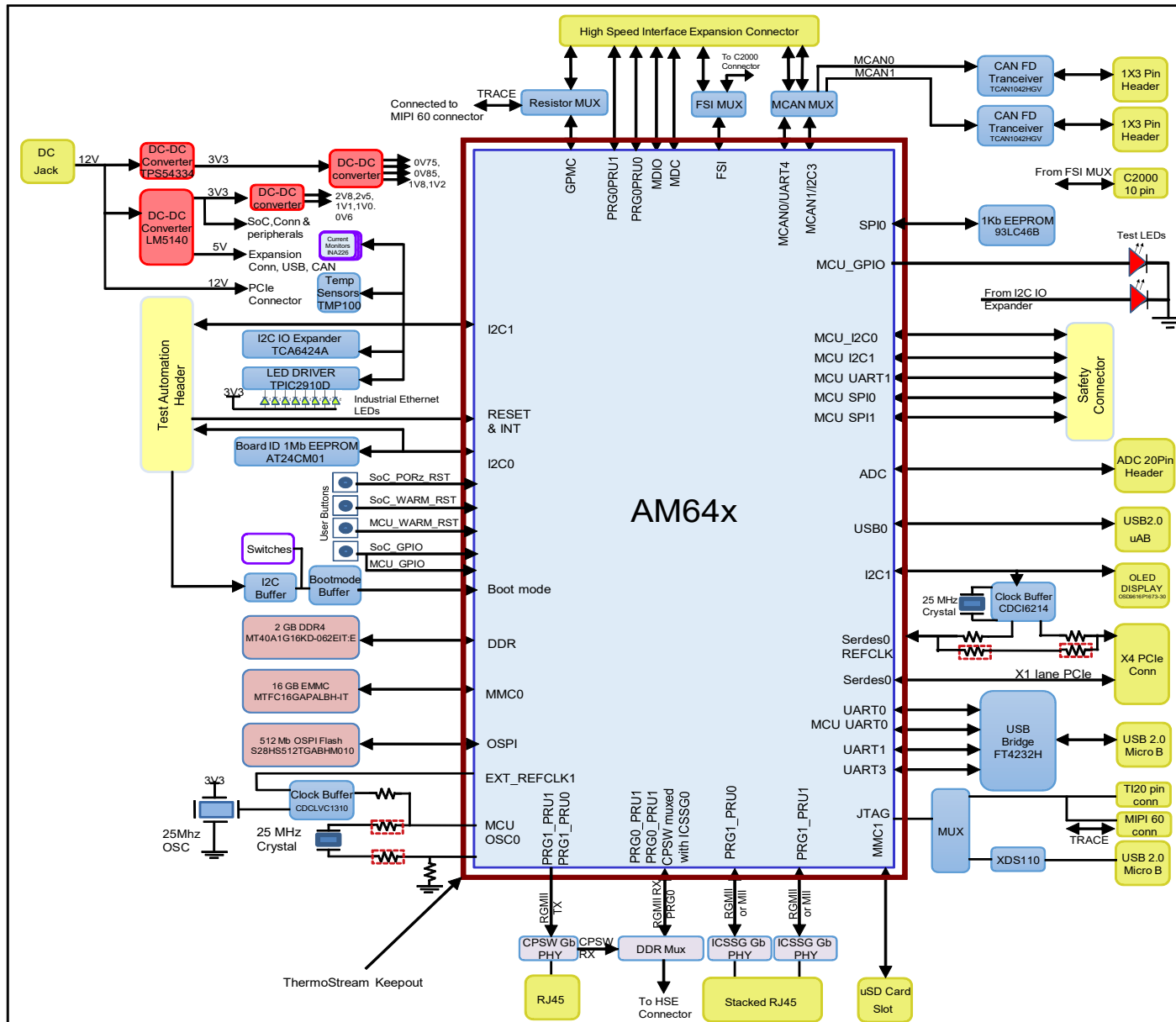
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Title REVISION HISTORY

Size	Variant Name = PROC101B(001) TMD564GPEVM	Rev
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BLOCK DIAGRAM_AM64x_EVM



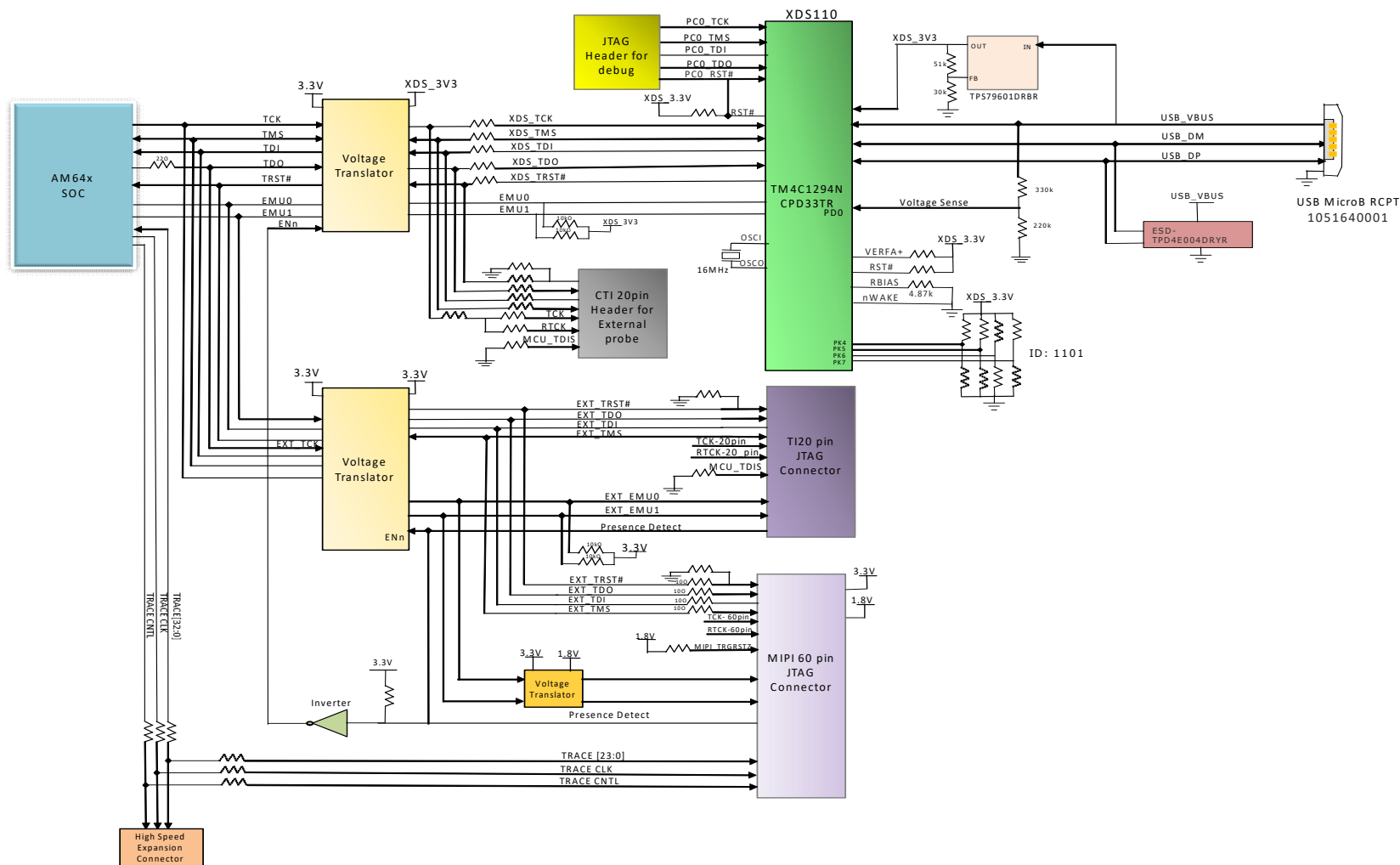
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Title BLOCK DIAGRAM_CP BOARD

Size	Variant Name = PROC101B(001) TMD564GPEVM	Rev
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BLOCK DIAGRAM_XDS110



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Title BLOCK DIAGRAM_XDS110

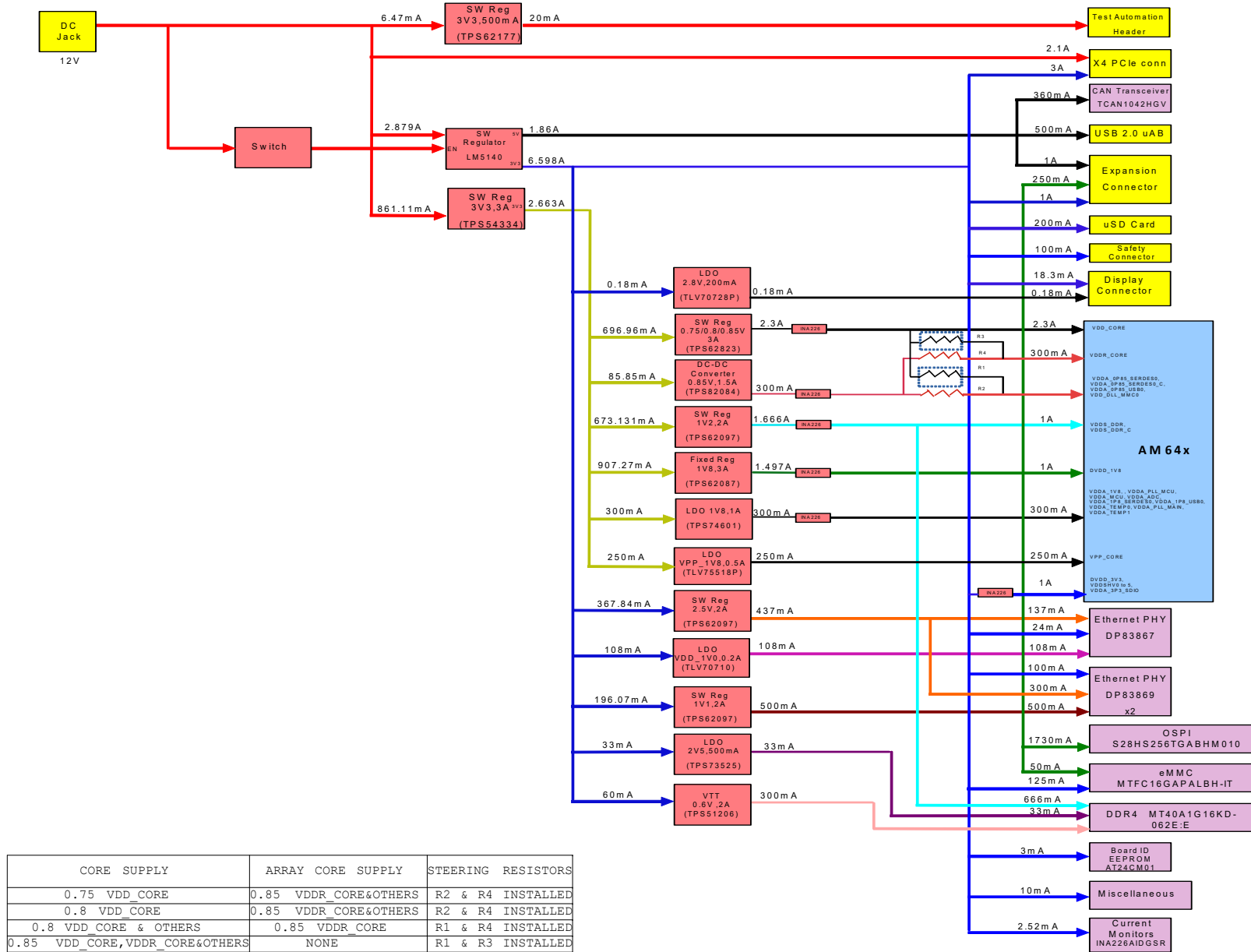
Size Variant Name = PROC101B(001) TMS64GPEVM

Date: Friday, March 26, 2021

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Rev E2

POWER FLOW DIAGRAM



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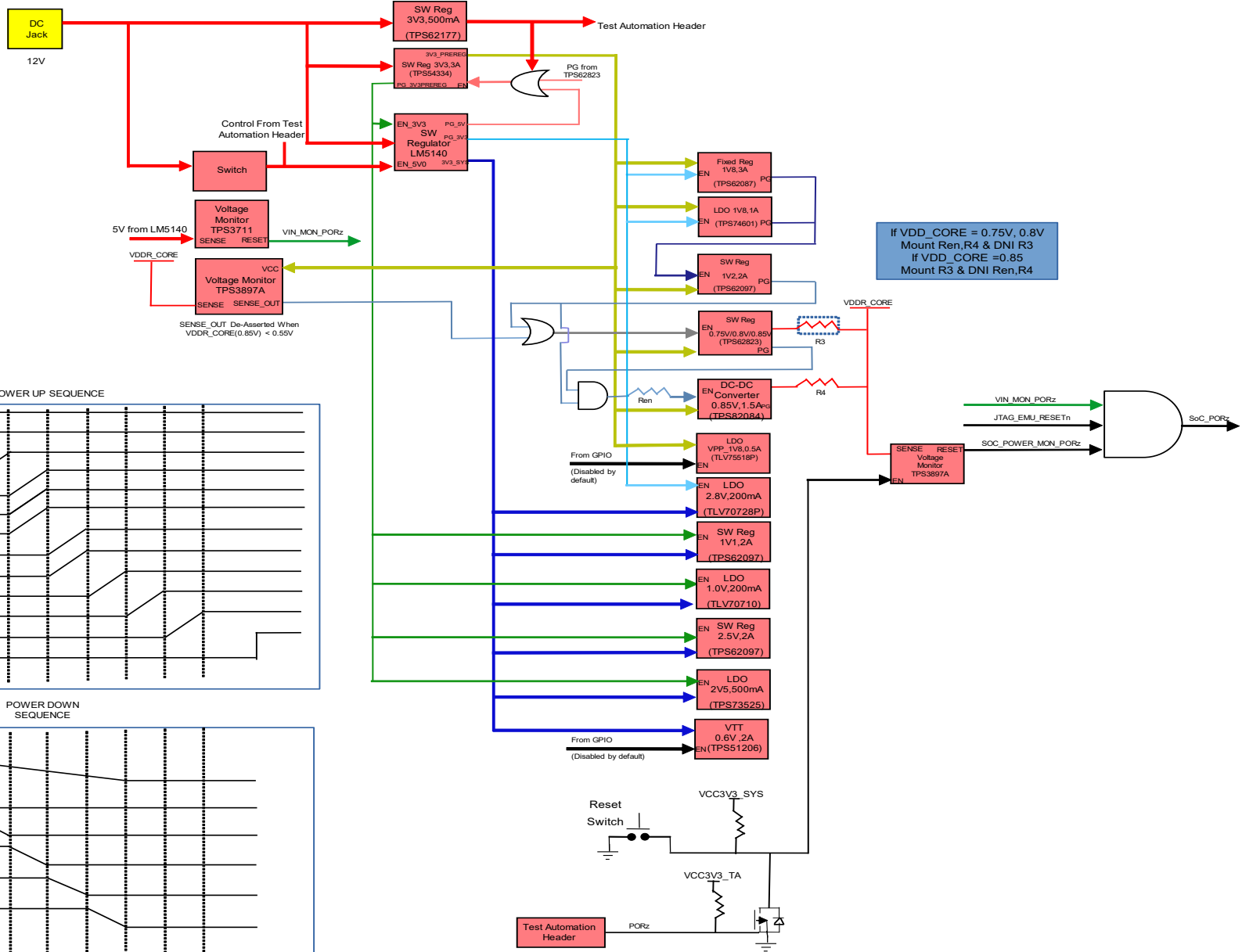


Title POWER FLOW DIAGRAM

Size Variant Name = PROC101B(001) TMS64GPEVM
 C Date: Friday, March 26, 2021
 Rev E2

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POWER SEQUENCE



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Title POWER SEQUENCE

Size	Variant Name = PROC101B(001) TMSD64GPEVM	Rev
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Date: Monday, May 10, 2021

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GPIO MAPPING TABLE

S.NO	GPIO DESCRIPTION	GPIO NETNAME	REQUIRED ON	FUNCTIONALITY	GPIO USED	SoC Muxed Signal Name	DIRECTION WITH RESPECT TO CONTROL	DEFAULT STATE	ACTIVE STATE
1	EMMC RESET Control GPIO	GPIO_eMMC_RSTn	GP EVM	Reset	IO EXPANDER- P00		OUTPUT	HIGH	LOW
2	OSPI RESET Control GPIO	GPIO_OSPI_RSTn	GP EVM	Reset	GPIO013	OSPI_CS2	OUTPUT	HIGH	LOW
3	CPSW RGMII1 RESET Control GPIO	GPIO_CPSW1_RST	GP EVM	Reset	IO EXPANDER- P02		OUTPUT	HIGH	LOW
4	PRG1 RGMII1 Ethernet PHY RESET Control GPIO	GPIO_RGMII1_RST	GP EVM	Reset	IO EXPANDER- P03		OUTPUT	HIGH	LOW
5	PRG1 RGMII2 Ethernet PHY RESET Control GPIO	GPIO_RGMII2_RST	GP EVM	Reset	IO EXPANDER- P04		OUTPUT	HIGH	LOW
6	PRG1 RGMII1 Ethernet PHY Link Detection GPIO	PRG1_ETH1_LED_LINK	GP EVM	Link Detection	PRG1_PRU0_GPO8		INPUT	LOW	HIGH
7	PRG1 RGMII2 Ethernet PHY Link Detection GPIO	PRG1_ETH2_LED_LINK	GP EVM	Link Detection	PRG1_PRU1_GPO8		INPUT	LOW	HIGH
8	CPSW Ethernet PHY Interrupt	CPSW_RGMII_INTn	GP EVM	Interrupt	Connected to PRG1_RGMII_INT via OE res		INPUT	HIGH	LOW
9	PRG1 Ethernet PHY 1Interrupt	PRG1_RGMII_INT	GP EVM	Interrupt	GPIO1_70	EXTINTn	INPUT	HIGH	LOW
10	PRG1 Ethernet PHY 2Interrupt			Interrupt			INPUT	HIGH	LOW
11	PCIe RESET Control GPIO	GPIO_PCl_e_RST_OUT	GP EVM	Reset	IO EXPANDER- P05		OUTPUT	LOW	HIGH
12	SD card load switch enable control	MMC1_SD_EN	GP EVM	Load SW Enable	IO EXPANDER- P06		OUTPUT	HIGH	LOW
13	One GPIO is required to control the Mux select between HSE and FSI Connector	FSI_FET_SEL	GP EVM	Mux Selection	IO EXPANDER- P07		OUTPUT	PREFERABLE	PREFERABLE
14	One GPIO is required to enable Standby mode in CAN transceiver	MCAN0_STB_3V3	GP EVM	Standby mode selection	IO EXPANDER- P10		OUTPUT	LOW	HIGH
15	One GPIO is required to enable Standby mode in CAN transceiver	MCAN1_STB_3V3	GP EVM	Standby mode selection	IO EXPANDER- P11		OUTPUT	LOW	HIGH
16	One GPIO is required to control the Mux select between HSE and Ethernet PHY	CPSW_FET_SEL	GP EVM	Mux Selection	IO EXPANDER- P12		OUTPUT	PREFERABLE	PREFERABLE
17	MDC/MDIO FET Switch Select for Mux	PRG1_RGMII2_FET_SEL	GP EVM	Mux Selection	IO EXPANDER- P14		OUTPUT	PREFERABLE	PREFERABLE
18	VTT 0.6V regulator Enable	VTT_EN	GP EVM	VTT 0.6V regulator Enable	GPIO0_12	OSPI0_CSn1	OUTPUT	LOW	HIGH
19	TEST GPIO1 from Test Automation Connector/ GPIO for GP board push button	TEST GPIO1/GPIO1_43	GP EVM	GPIO for communications with AM64x	GPIO1_43	SPI0_CS1	INPUT	HIGH	LOW
20	TEST GPIO2 from Test Automation Connector	TEST GPIO2	GP EVM	GPIO for communications with AM64x	IO EXPANDER- P15		INPUT	HIGH	LOW
21	OLED Display RESET GPIO	GPIO_OLED_RESETn	GP EVM	Reset	IO EXPANDER- P16		OUTPUT	LOW	HIGH
22	IO Expander Interrupt	IO_EXP_INTn	GP EVM	Interrupt	GPIO1_78	MMC1_SDWP	INPUT	HIGH	LOW
23	VPP 1.8V regulator Enable	VPP_LDO_EN	GP EVM	VPP 0.1.8V regulator Enable	IO EXPANDER- P17		OUTPUT	LOW	HIGH
24	One GPIO is required to control the Mux select between HSE and CAN Interface	CAN_MUX_SEL	GP EVM	Mux Selection	IO EXPANDER- P01		OUTPUT	LOW	HIGH
25	User LED	TEST_LED1	GP EVM	Test	IO EXPANDER- P20		OUTPUT	LOW	HIGH
26	User LED	TEST_LED2	GP EVM	Test	MCU_SPI1_CS0	MCU_GPIO0_5	OUTPUT	LOW	HIGH
27	One GPIO to enable the PCIe Clock generator outputs	CDC_OE1/E4	GP EVM	Clock output enable	IO EXPANDER- P21		OUTPUT	HIGH	HIGH

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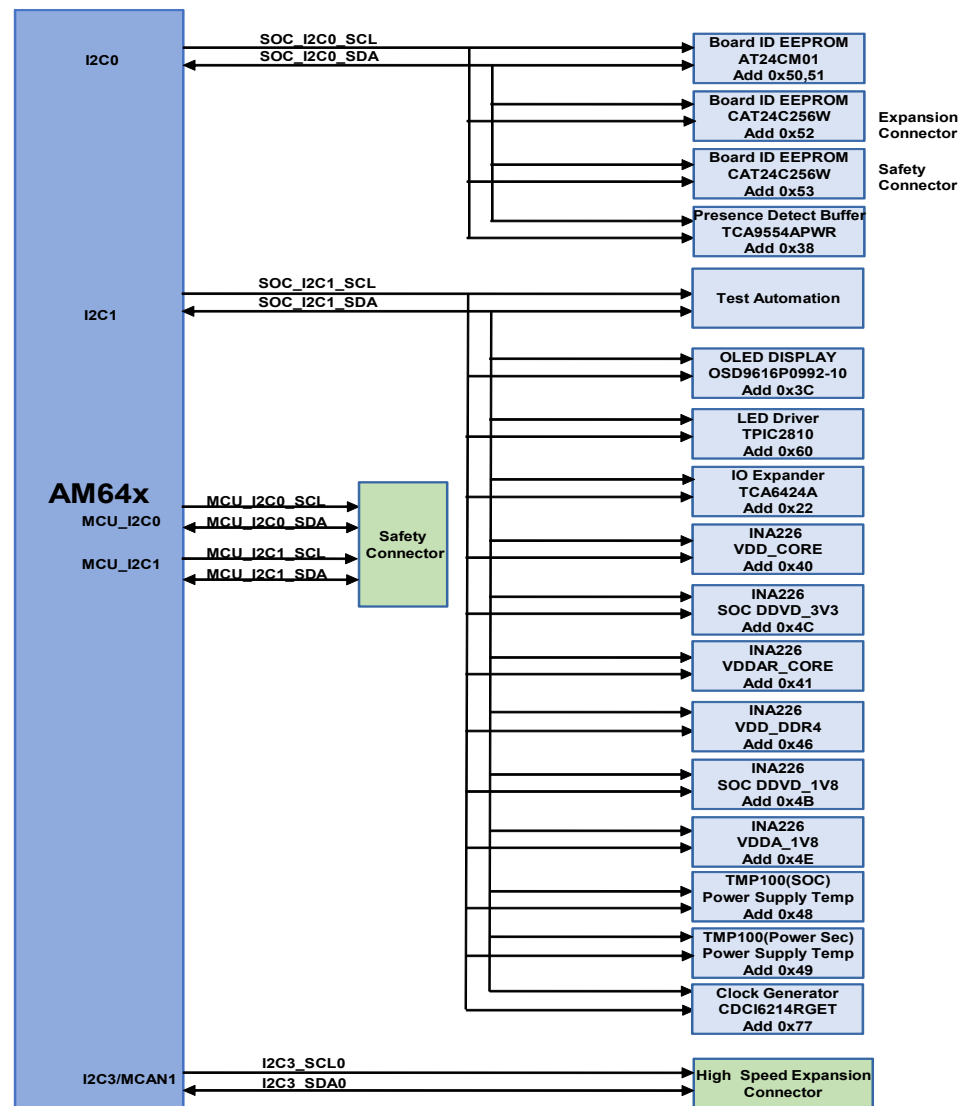
Title GPIO_MAPPING TABLE

Size Variant Name = PROC101B(001) TMD564GPEVM

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I2C TREE



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Title I2C TREE

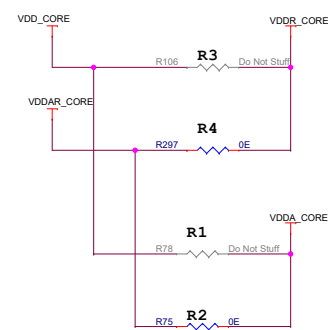
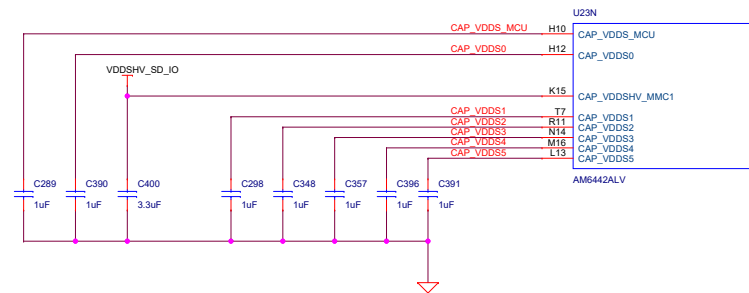
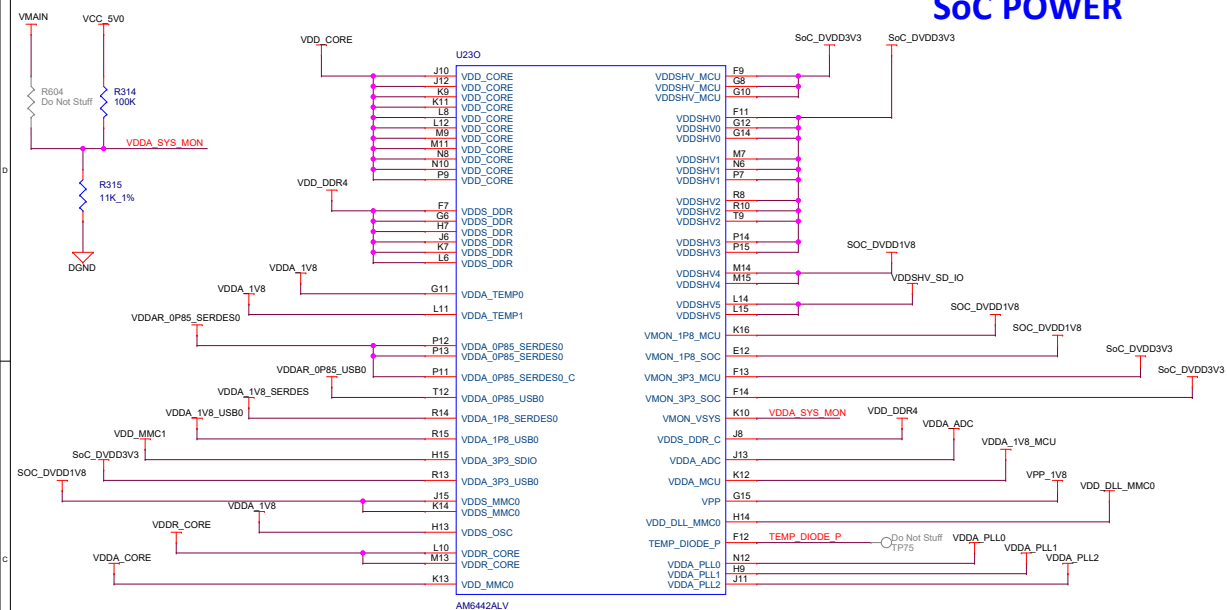
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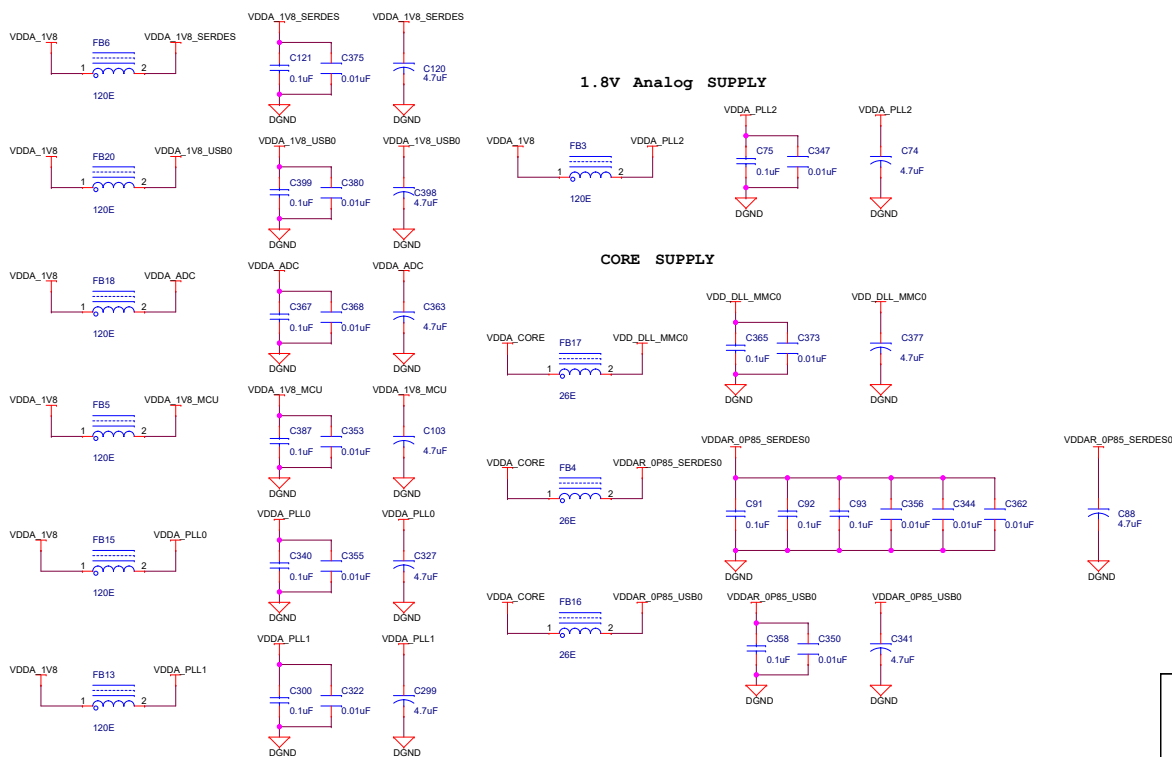
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SoC POWER



1.8V Analog SUPPLY



CORE SUPPLY	ARRAY CORE SUPPLY	STEERING RESISTORS
0.75 VDD CORE	0.85 VDDR CORE&OTHERS	R2 & R4 INSTALLED
0.8 VDD CORE	0.85 VDDR CORE&OTHERS	R2 & R4 INSTALLED
0.8 VDD CORE & OTHERS	0.85 VDDR CORE	R1 & R4 INSTALLED
0.85 VDD CORE,VDDR CORE&OTHERS	NONE	R1 & R3 INSTALLED

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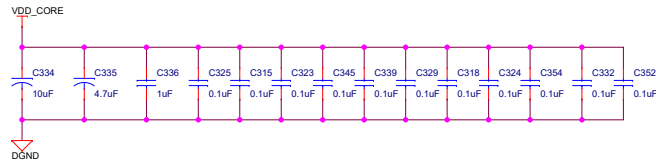


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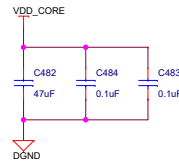
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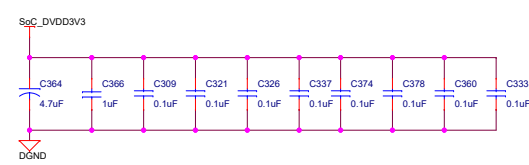
SoC POWER Decaps



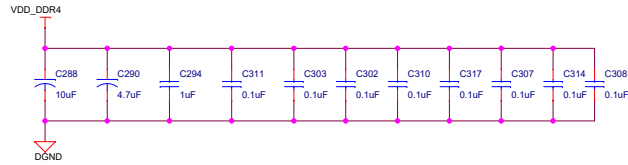
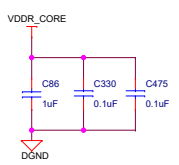
Place one 0.1uF cap near each Pin



To place after current sense resistor on VDD_CORE plane

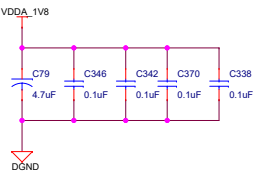


Place one 0.1uF cap near each Pin

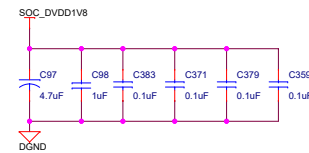
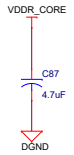
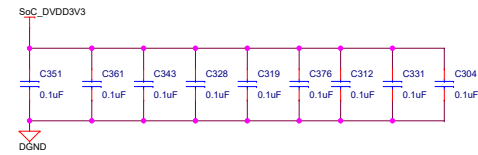
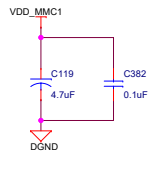


VDD ARRAY CORE

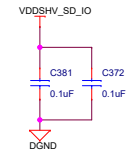
VDDA_3P3_SDIO



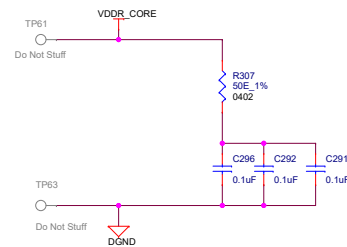
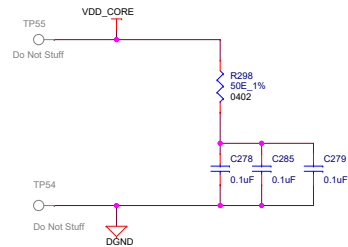
Place one 0.1uF cap near each Pin



Place one 0.1uF cap near each Pin



Core & Array Core Supply Kelvin Sensing



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Title SOC POWER CAPS

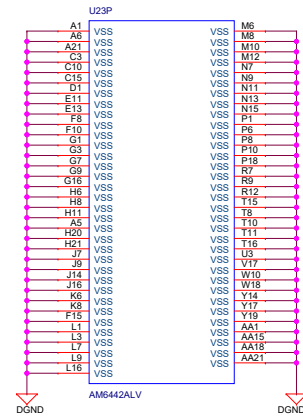
Size Variant Name = PROC101B(001) TMS64GPEVM

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SoC POWER - VSS



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Title SOC VSS

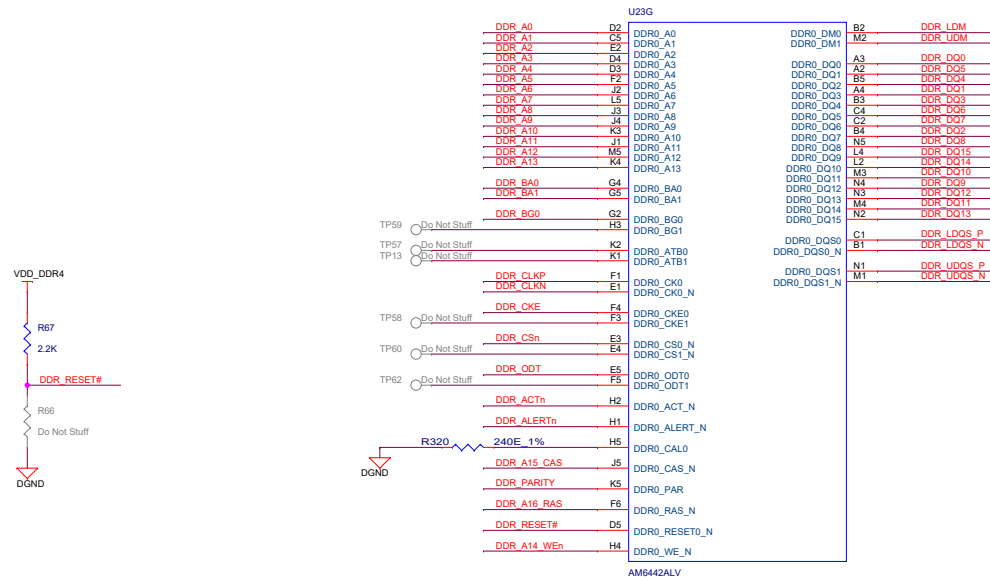
Size Variant Name = PROC101B(001) TMD564GPEVM

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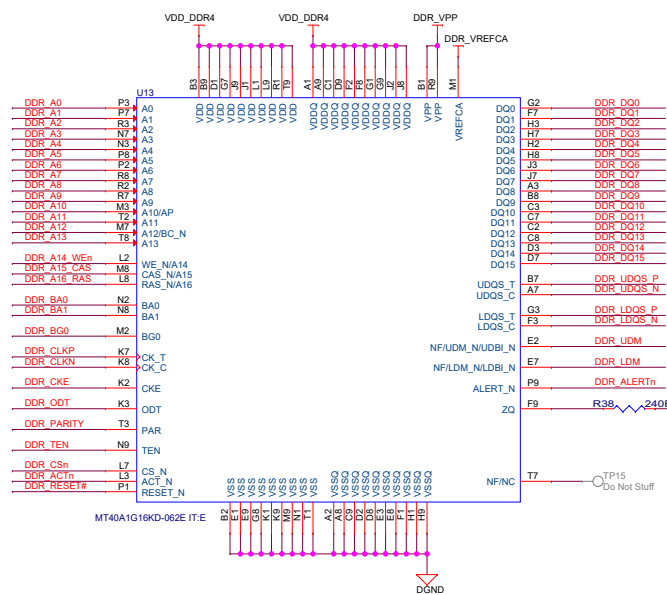
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SoC DDR INTERFACE

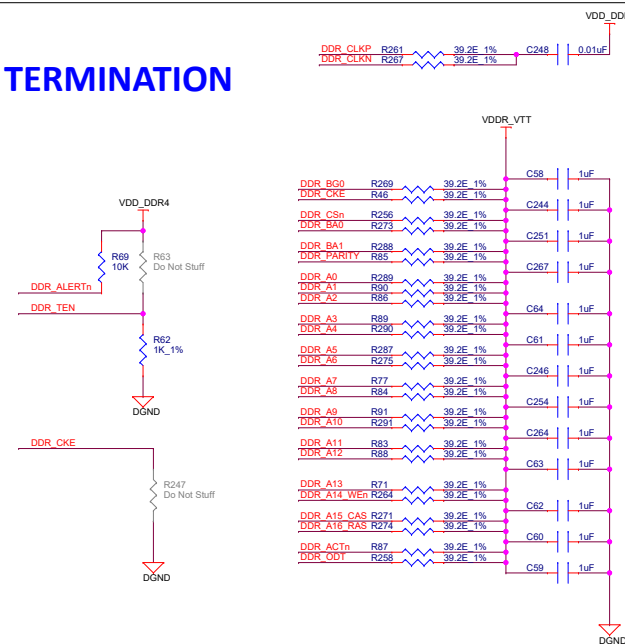


DDR DQ Lines Swapped
With Data Byte

DDR4 DEVICE



DDR TERMINATION



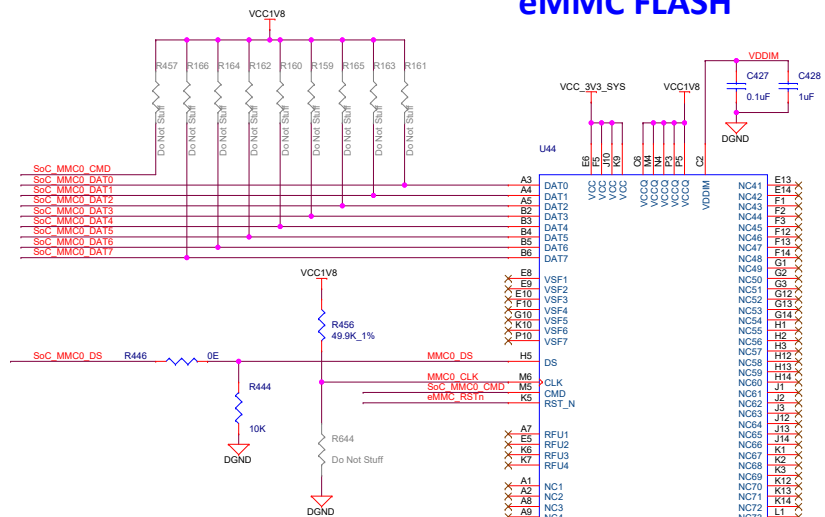
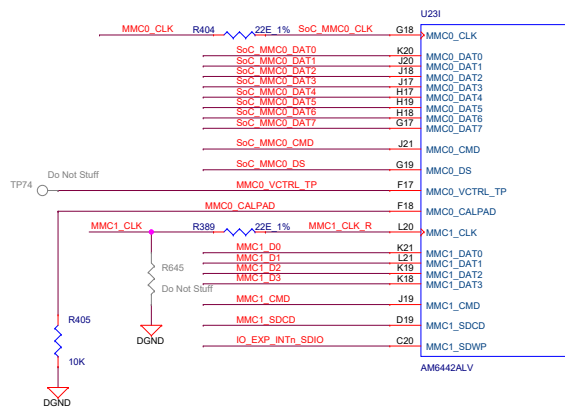
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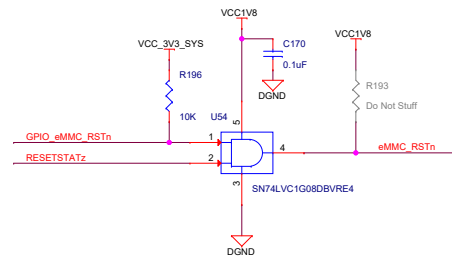
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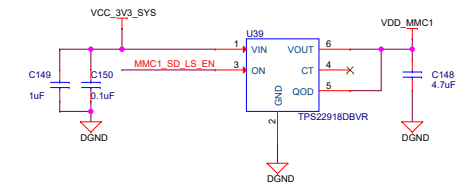
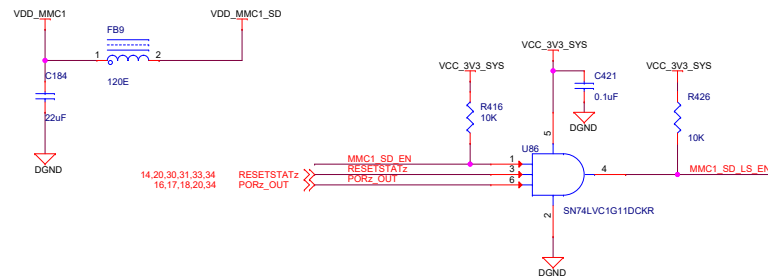
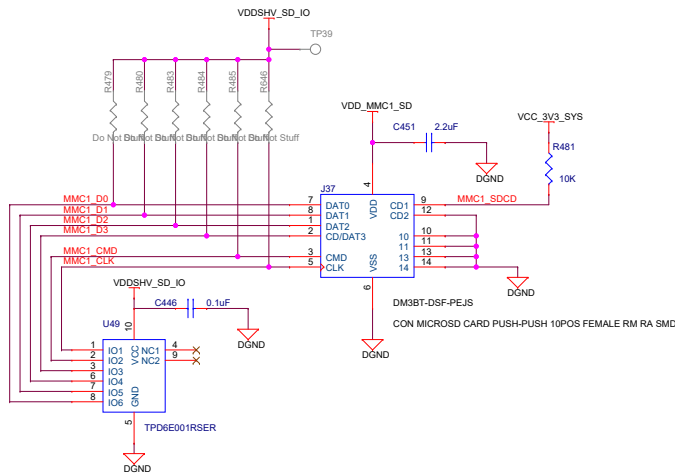
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eMMC FLASH RESET



SD CARD INTERFACE



Off Page Connections

From 4	33	IO_EXP_INTn_SDIO	IO_EXP_INTn_SDIO
To IO Expander	33	GPIO_eMMC_RSTn	GPIO_eMMC_RSTn
	33	MMC1_SD_EN	MMC1_SD_EN

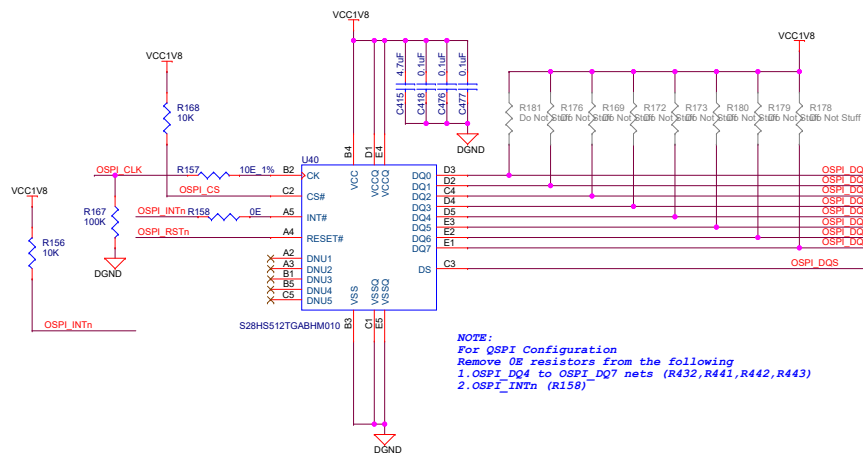
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Title eMMC FLASH_SDCARD INTERFACE

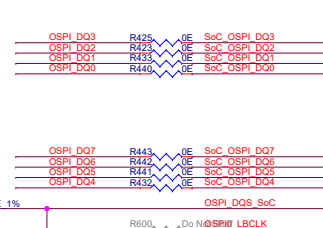
Size	Variant Name = PROC101B(001) TMS64GPEVM	Rev
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OSPI FLASH

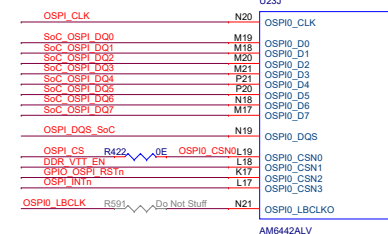


NOTE:
For QSPI Configuration
Remove 0E resistors from the following
1.OSPI_DQ4 to OSPI_DQ7 nets (R432,R441,R442,R443)
2.OSPI_INTn (R158)

SOC OSPI INTERFACE



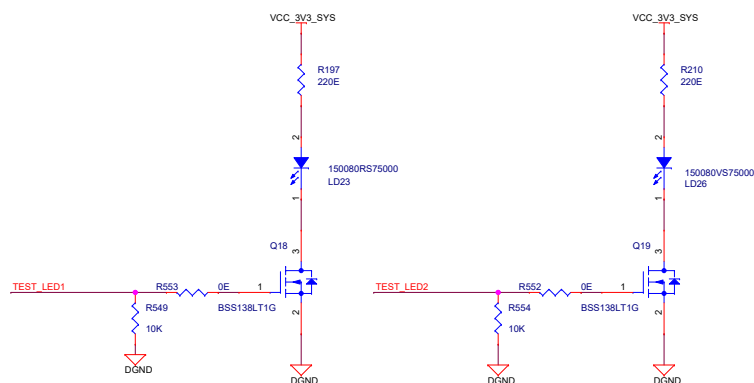
Place R600 close to the memory to avoid stub



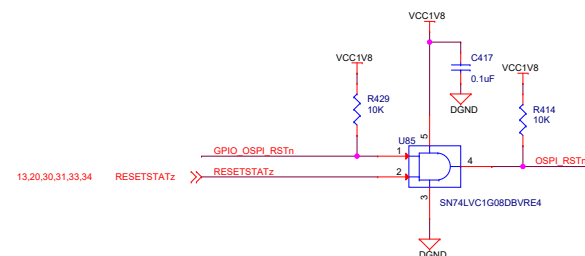
Place R591 close to the ball
with as little trace as possible

To Route DQS to LBCLK0	To Route DQS to SOC's DQS
Mount R591 & R600	Mount R601 & R592
DNI R601 & R592	DNI R591 & R600

USER TEST LED



OSPI FLASH RESET



Off Page Connections

To Level Translator

1 Page connections

TEST_LED1	«	TEST_LED1	33
TEST_LED2	«	TEST_LED2	34
DDR_VTT_EN	»	DDR_VTT_EN	33

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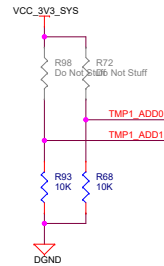


	Title	OSPI
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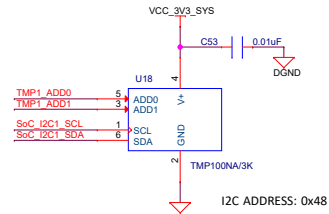
Size	Variant Name = PROC101B(001) TMDS64GPEVM
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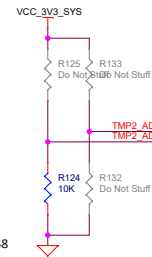
TEMPERATURE SENSOR



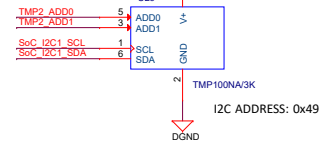
NOTE: PLACE TEMP SENSOR CLOSE TO SoC



I2C ADDRESS: 0x48



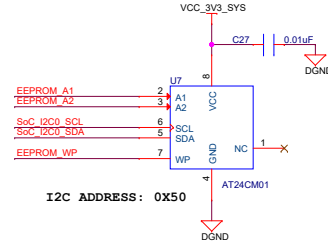
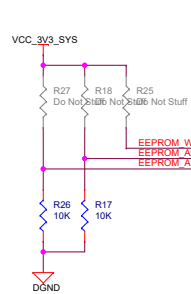
NOTE: PLACE TEMP SENSOR CLOSE TO CORE POWER SECTION



I2C ADDRESS: 0x49

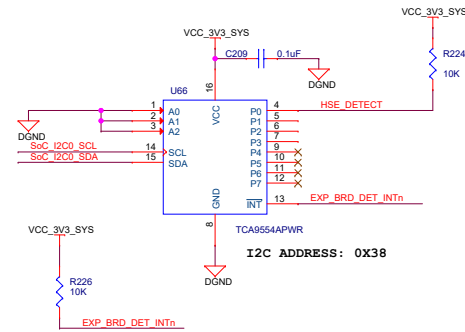


BOARD ID EEPROM



I2C ADDRESS: 0x50

BOARD PRESENCE DETECT CIRCUIT



I2C ADDRESS: 0x38

Off Page Connections

HSE_DETECT	HSE_DETECT	27
SoC_I2C1_SDA	SoC_I2C1_SDA	19,21,29,30,31,32,33
SoC_I2C1_SCL	SoC_I2C1_SCL	19,21,29,30,31,32,33
SoC_I2C0_SDA	SoC_I2C0_SDA	27,29,33
SoC_I2C0_SCL	SoC_I2C0_SCL	27,29,33

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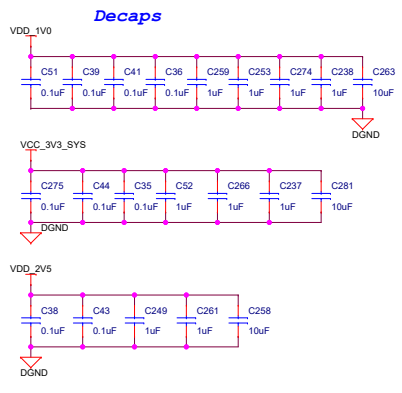
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Size Variant Name = PROC101B(001) TMD564GPEVM

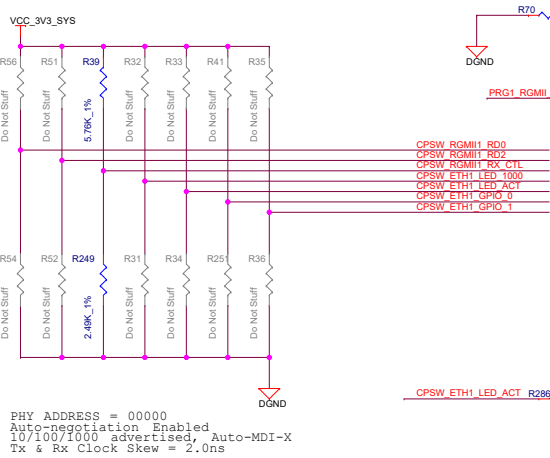
Date: Friday, March 26, 2021

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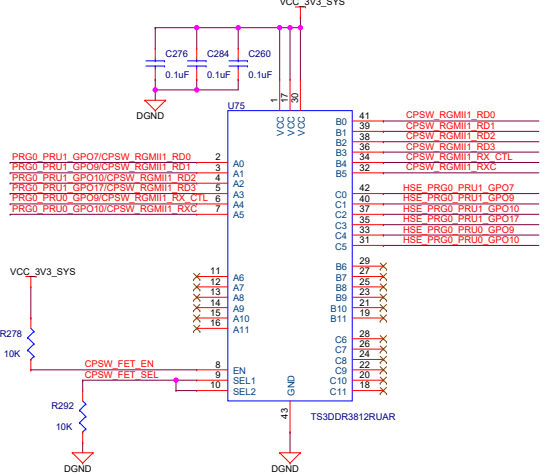
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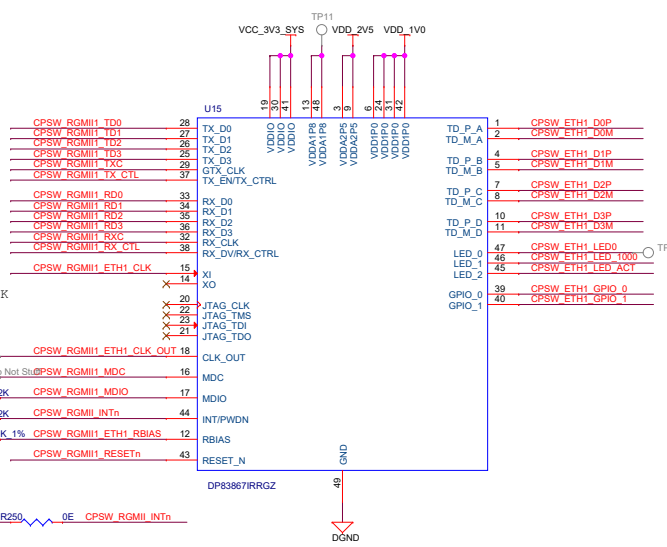
STRAPPING RESISTORS



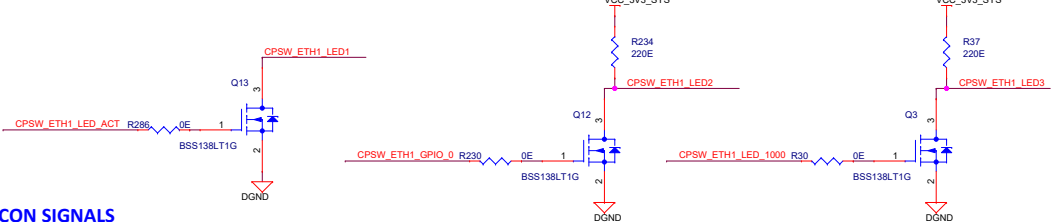
CPSW RGMII 1 ETHERNET PHY SIGNALS & HSE CON SIGNALS



CPSW RGMII 1 - PHY



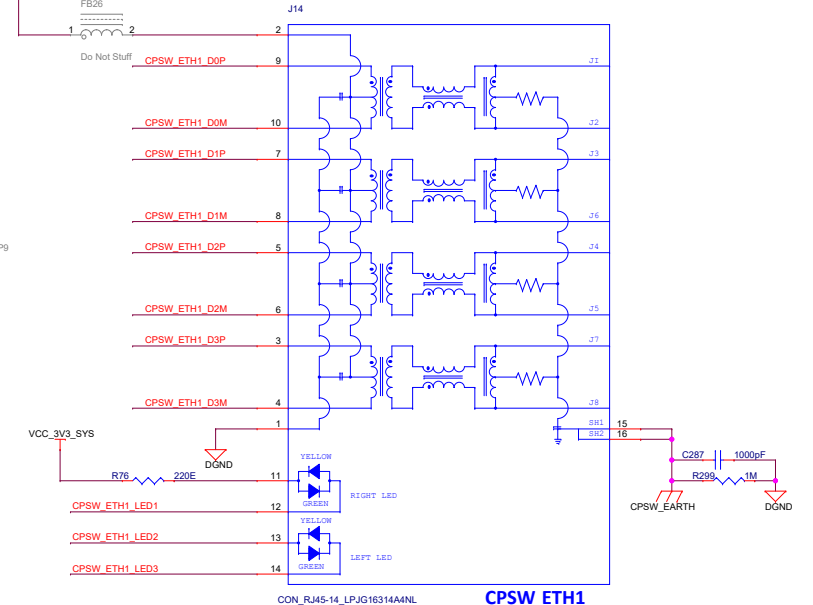
CPSW_ETHERNET PHY-1 SPEED & ACTIVITY LED's DRIVERS



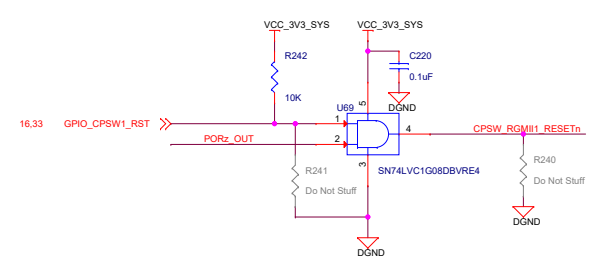
TS3DDR3812RUAR Truth Table

EN	SEL1	SEL2	FUNCTION
L	X	X	A0 to A11, B0 to B11, and C0 to C11 are Hi-Z
H	L	L	A0 to A5 = B0 to B5 and A6 to A11 = B6 to B11
H	L	H	A0 to A5 = B0 to B5 and A6 to A11 = C6 to C11
H	H	L	A0 to A5 = C0 to C5 and A6 to A11 = B6 to B11
H	H	H	A0 to A5 = C0 to C5 and A6 to A11 = C6 to C11

RJ45 with Integrated Magnetics



CPSW ETH1 RESET



Off Page Connections

From	To
Processor	PRG0_PRU1_GPO7/CPSW_RGMII1_RD0, PRG0_PRU1_GPO9/CPSW_RGMII1_RD1, PRG0_PRU1_GPO10/CPSW_RGMII1_RD2, PRG0_PRU1_GPO17/CPSW_RGMII1_RD3, PRG0_PRU0_GPO9/CPSW_RGMII1_RX_CTL, PRG0_PRU0_GPO10/CPSW_RGMII1_RXC
Processor	CPSW_RGMII1_TD0, CPSW_RGMII1_TD1, CPSW_RGMII1_TD2, CPSW_RGMII1_TD3, CPSW_RGMII1_TX_CTL, CPSW_RGMII1_TXC
IO Expander	GPIO_CPSW1_RST, CPSW_FET_SEL
Clock Buffer	CPSW_RGMII1_ETH1_CLK
HSE Connector	HSE_PRG0_PRU1_GPO7, HSE_PRG0_PRU1_GPO9, HSE_PRG0_PRU1_GPO10, HSE_PRG0_PRU1_GPO17, HSE_PRG0_PRU1_GPO19, HSE_PRG0_PRU0_GPO9, HSE_PRG0_PRU0_GPO10
Processor	CPSW_RGMII1_MDIO, CPSW_RGMII1_MDC

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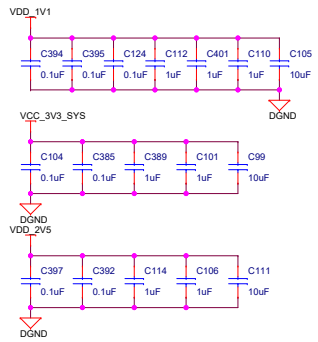


Title			CPSW RGMII_1 ETHERNET PHY		
Size	Variant Name	Rev			
C	PROC1019(B01)TMD984GPEVM	E2			
Date	Friday, September 03, 2021	Sheet	16	of	40

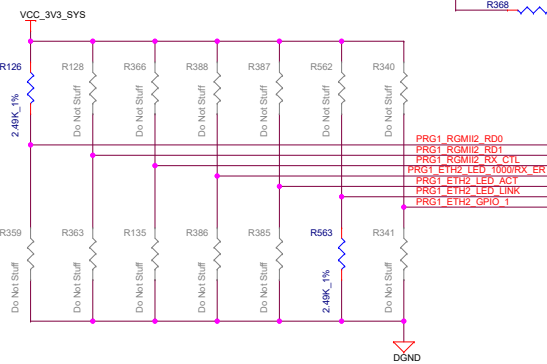
ICSSG1 - RGMII 2

Dual RJ45 CON With Integrated Magnetics

Decaps

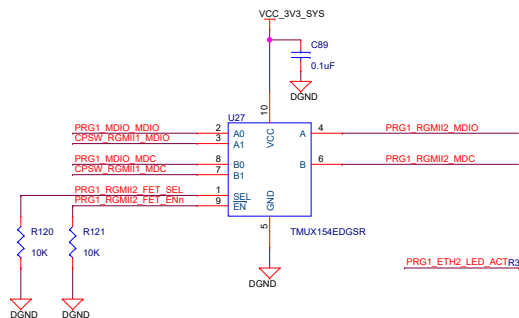


STRAPPING RESISTORS



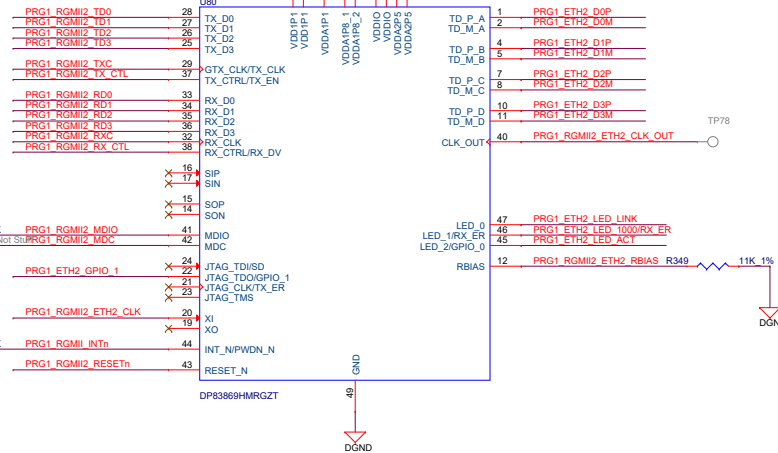
PHY ADDRESS = 00011
Auto-negotiation, 10/100/1000 advertised, Auto-MDI-X
RGMII to Copper (1000Base-T/100Base-TX/10Base-T)

PRG1 MDC/MDIO FET SWITCH

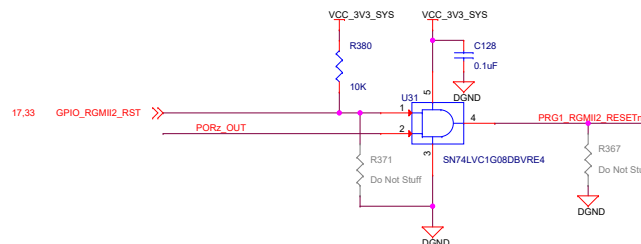


TMUX154EDGSR Truth Table

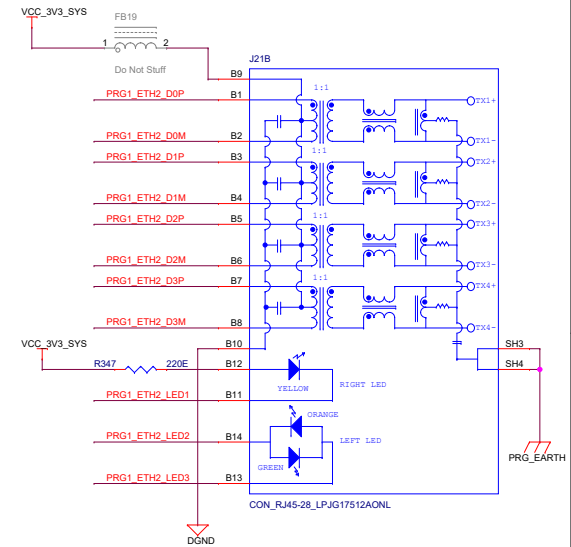
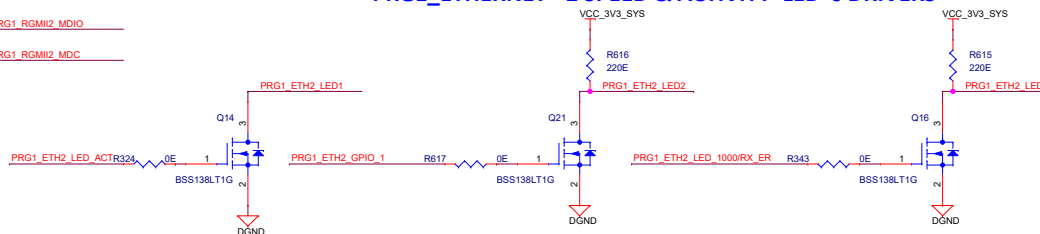
SEL	EN	FUNCTION
X	H	Disconnect
L	L	A = A0 B = B0
H	L	A = A1 B = B1



PRG1 ETH2 RESET



PRG1_ETHERNET - 2 SPEED & ACTIVITY LED's DRIVERS



Off Page Connections

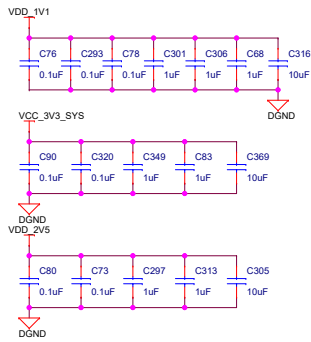
To Processor	16,18,34	PRG1_RGMII_INTn	PRG1_RGMII_INTn
	27	PRG1_RGMII2_RD0	PRG1_RGMII2_RD0
	27	PRG1_RGMII2_RD1	PRG1_RGMII2_RD1
	27	PRG1_RGMII2_RD2	PRG1_RGMII2_RD2
	27	PRG1_RGMII2_RD3	PRG1_RGMII2_RD3
	27	PRG1_RGMII2_RXC	PRG1_RGMII2_RXC
	27	PRG1_RGMII2_RX_CTL	PRG1_RGMII2_RX_CTL
	27	PRG1_ETH2_LED_LINK	PRG1_ETH2_LED_LINK
	27	PRG1_ETH2_LED_1000RX_ER	PRG1_ETH2_LED_1000RX_ER
From Processor	27	PRG1_RGMII2_TD0	PRG1_RGMII2_TD0
	27	PRG1_RGMII2_TD1	PRG1_RGMII2_TD1
	27	PRG1_RGMII2_TD2	PRG1_RGMII2_TD2
	27	PRG1_RGMII2_TD3	PRG1_RGMII2_TD3
	27	PRG1_RGMII2_TXC	PRG1_RGMII2_TXC
	27	PRG1_RGMII2_TX_CTL	PRG1_RGMII2_TX_CTL
	13,16,18,20,34	PORz_OUT	PORz_OUT
	18,27	PRG1_MDIO_MDIO	PRG1_MDIO_MDIO
	18,27	PRG1_MDIO_MDC	PRG1_MDIO_MDC
From CPSW SW	16,27	CPSW_RGMII1_MDIO	CPSW_RGMII1_MDIO
	16,27	CPSW_RGMII1_MDC	CPSW_RGMII1_MDC
From IO Expander	17,33	GPIO_RGMII2_RST	GPIO_RGMII2_RST
	33	PRG1_RGMII2_FET_SEL	PRG1_RGMII2_FET_SEL
From Clock Buffer	31	PRG1_RGMII2_ETH2_CLK	PRG1_RGMII2_ETH2_CLK

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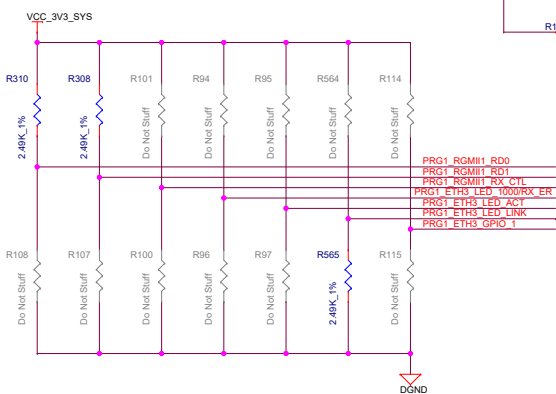


Title	ICSSG1 RGMII_2 ETHERNET PHY	
Size	Variant Name = PROC101B(001) TMD964GPEVM	Rev
C		E2
Date:	Friday, March 26, 2021	Sheet 17 of 40

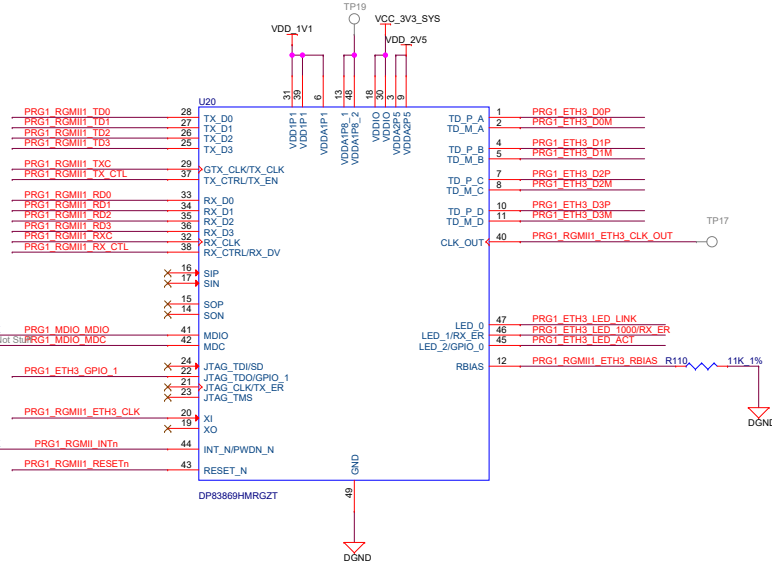
Decaps



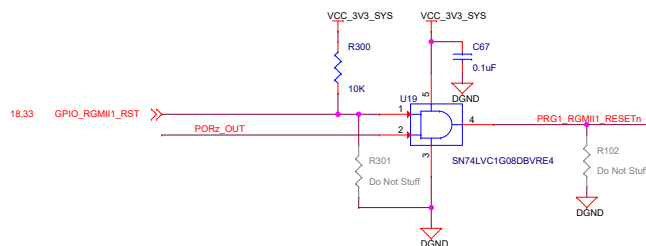
STRAPPING RESISTORS



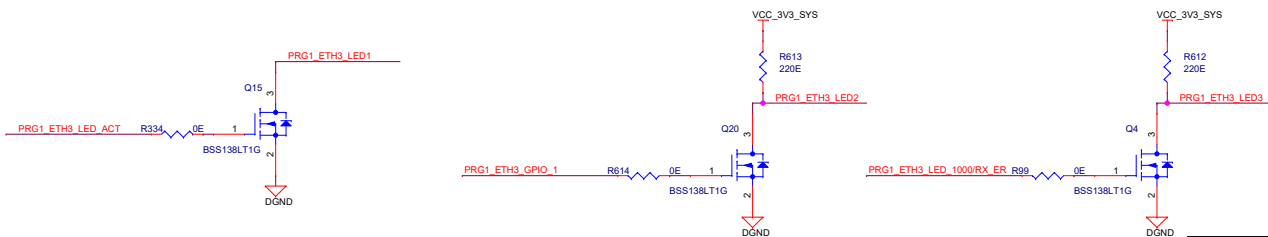
```
PHY ADDRESS = 01111
Auto-negotiation, 10/100/1000 advertised, Auto-MDI-X
RGMII to Copper (1000BaseT/100Base-TX/10Base-T)
```



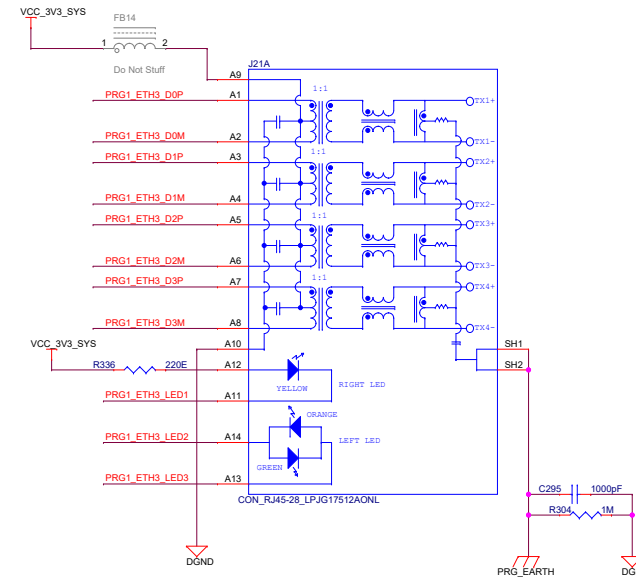
PRG1 ETH2 RESET



PRG1_ETHERNET - 3 SPEED & ACTIVITY LED 's DRIVERS



Dual RJ45 CON With Integrated Magnetics



Off Page Connections

To Processor	16,17,34	PRG1_RGMII_INTn	↔	PRG1_RGMII_INTn
	17,37	PRG1_RGMII_RD0	↔	PRG1_RGMII_RD0
	27	PRG1_RGMII_RD1	↔	PRG1_RGMII_RD1
	27	PRG1_RGMII_RD2	↔	PRG1_RGMII_RD2
	27	PRG1_RGMII_RD3	↔	PRG1_RGMII_RD3
	27	PRG1_RGMII_RD0	↔	PRG1_RGMII_RXC
	27	PRG1_RGMII_RXC	↔	PRG1_RGMII_RXC
	27	PRG1_RGMII_RX_CTL	↔	PRG1_RGMII_RX_CTL
	13,16,17,20,34	PORZ_OUT	↔	PORZ_OUT
	27	PRG1_ETH3_LED_LINK	↔	PRG1_ETH3_LED_LINK
	27	PRG1_ETH3_LED_1000RX_ER	↔	PRG1_ETH3_LED_1000RX_ER
From Processor	27	PRG1_RGMII_TD0	↔	PRG1_RGMII_TD0
	27	PRG1_RGMII_TD1	↔	PRG1_RGMII_TD1
	27	PRG1_RGMII_TD2	↔	PRG1_RGMII_TD2
	27	PRG1_RGMII_TD3	↔	PRG1_RGMII_TD3
	27	PRG1_RGMII_TXC	↔	PRG1_RGMII_TXC
	27	PRG1_RGMII_TX_CTL	↔	PRG1_RGMII_TX_CTL
From Processor	17,27	PRG1_MDIO_MDIO	↔	PRG1_MDIO_MDIO
MDIO Pins are common to both PWR. This to be verified)	1,2,7	PRG1_MDIO_MDC	↔	PRG1_MDIO_MDC
From IO Expander	18,33	GPIO_RGMII_RST	↔	GPIO_RGMII_RST
From Clock Buffer	31	PRG1_RGMII_ETH3_CLK	↔	PRG1_RGMII_ETH3_CLK

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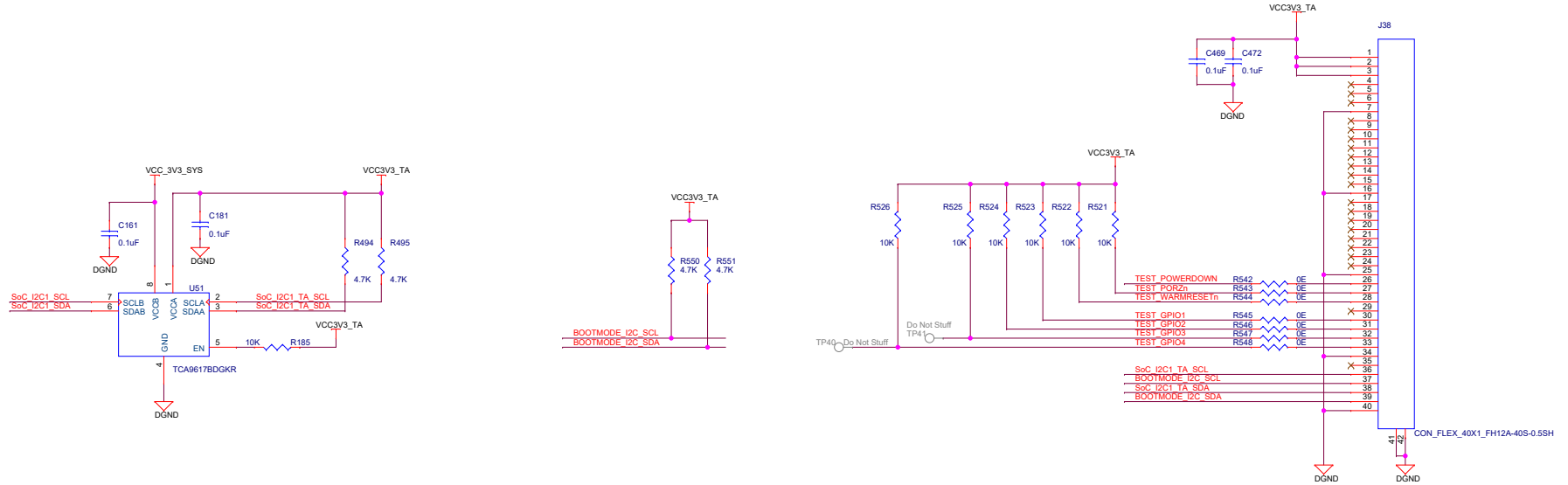


Title	ICSSG2 RGMII_1 ETHERNET PHY
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Size	Variant Name = PROC101B(001) TMS64GPEVM	Rev
C		E2
Date:	Friday, March 26, 2021	Sheet 18 of 40

TEST AUTOMATION

40-PIN AUTOMATION HEADER



TEST AUTOMATION GPIO MAPPING

SIGNAL NAME	DESCRIPTION	Direction WRT CTRL	Internal/ External PU/PD states
TEST_POWERDOWN	Used to Power down the OVP Circuit	OUTPUT	External Pullup
TEST_PORZn	Used to Reset the SoC PORz	OUTPUT	External Pullup
TEST_WARMRESETn	Used to Reset the SoC Warmreset	OUTPUT	External Pullup
TEST_GPIO1	Used to Generate the interrupt on GPIO0_13_INTn Pin	OUTPUT	External Pullup
TEST_GPIO2	Connected to I/O Expander to Communicate with SoC	OUTPUT	External Pullup
TEST_GPIO3	Used to Enable the BOOTMODE Buffer	OUTPUT	External Pullup
TEST_GPIO4	Used to Reset the Bootmode IO Expander	OUTPUT	External Pullup

Off Page Connections

To Processor	15,21,29,30,31,32,33	SoC_I2C1_SCL	SoC_I2C1_SCL
	15,21,29,30,31,32,33	SoC_I2C1_SDA	SoC_I2C1_SDA
To Bootmode Buffer	20	BOOTMODE_I2C_SCL	BOOTMODE_I2C_SCL
	20	BOOTMODE_I2C_SDA	BOOTMODE_I2C_SDA
To Debounce Ckt	35	TEST_PORZn	TEST_PORZn
To High Side SW	37	TEST_POWERDOWN	TEST_POWERDOWN
To Debounce Ckt	35	TEST_WARMRESETn	TEST_WARMRESETn
To Debounce Ckt	33	TEST_GPIO1	TEST_GPIO1
To IO Expander	35	TEST_GPIO2	TEST_GPIO2
To EN Boot Mode Buffer	20	TEST_GPIO3	TEST_GPIO3
To RST Boot Mode Buffer	20	TEST_GPIO4	TEST_GPIO4

Designed for TI by Mistral Solutions Pvt Ltd

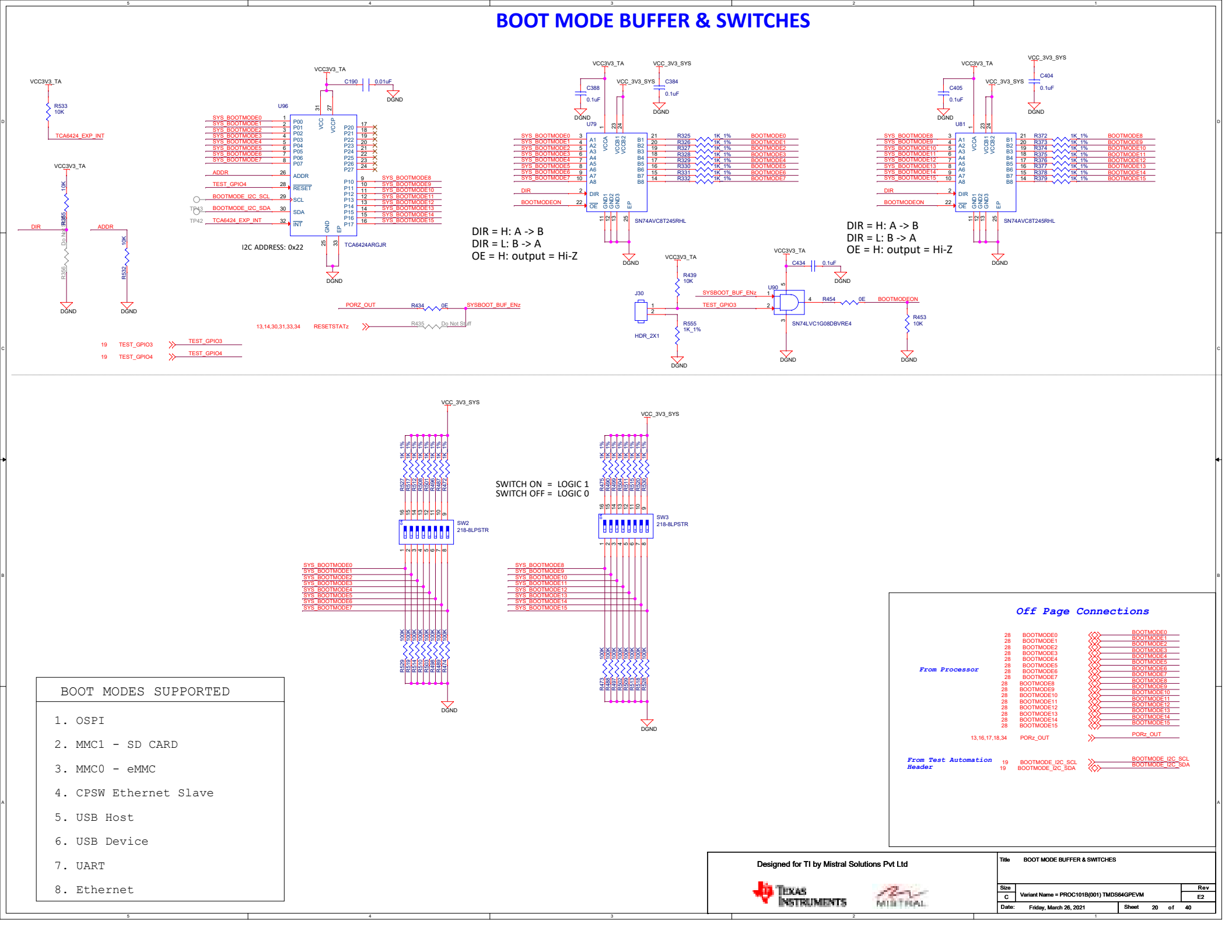
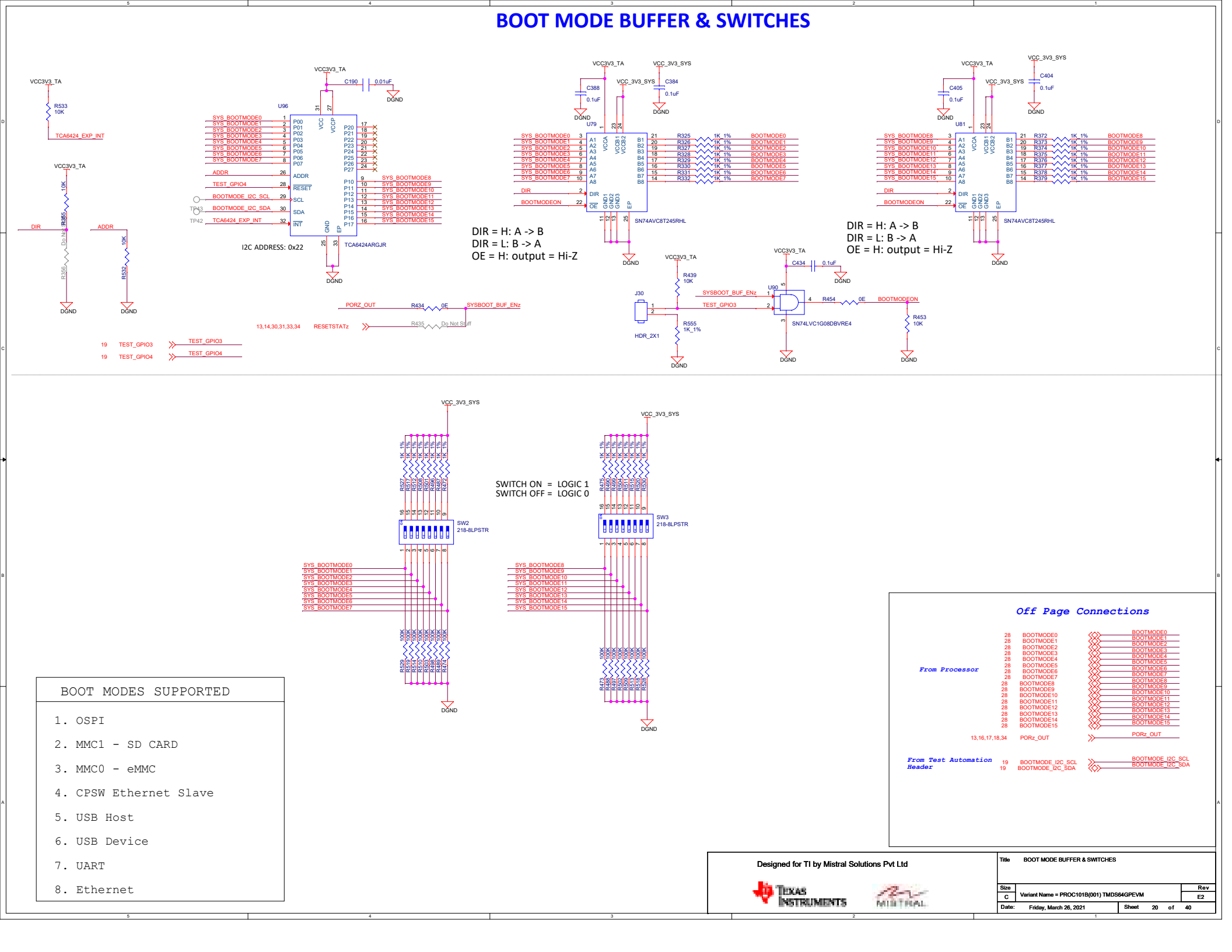


Title TEST AUTOMATION

Size Variant Name = PROC101B(001) TMS64GPEVM

Date: Friday, March 26, 2021 Sheet 19 of 40

Rev E2

[illegible]

BOOT MODE BUFFER & SWITCHES

- BOOT MODE BUFFER & SWITCHES

BOOT MODE BUFFER & SWITCHES

19 TEST_GPIO3 >>> TEST_GPIO3
19 TEST_GPIO4 >>> TEST_GPIO4

DIR = H: A -> B
DIR = L: B -> A
OE = H: output = Hi-Z

DIR = H: A -> B
DIR = L: B -> A
OE = H: output = Hi-Z

SWITCH ON = LOGIC 1
SWITCH OFF = LOGIC 0

SWITCH ON = LOGIC 1
SWITCH OFF = LOGIC 0

BOOT MODES SUPPORTED

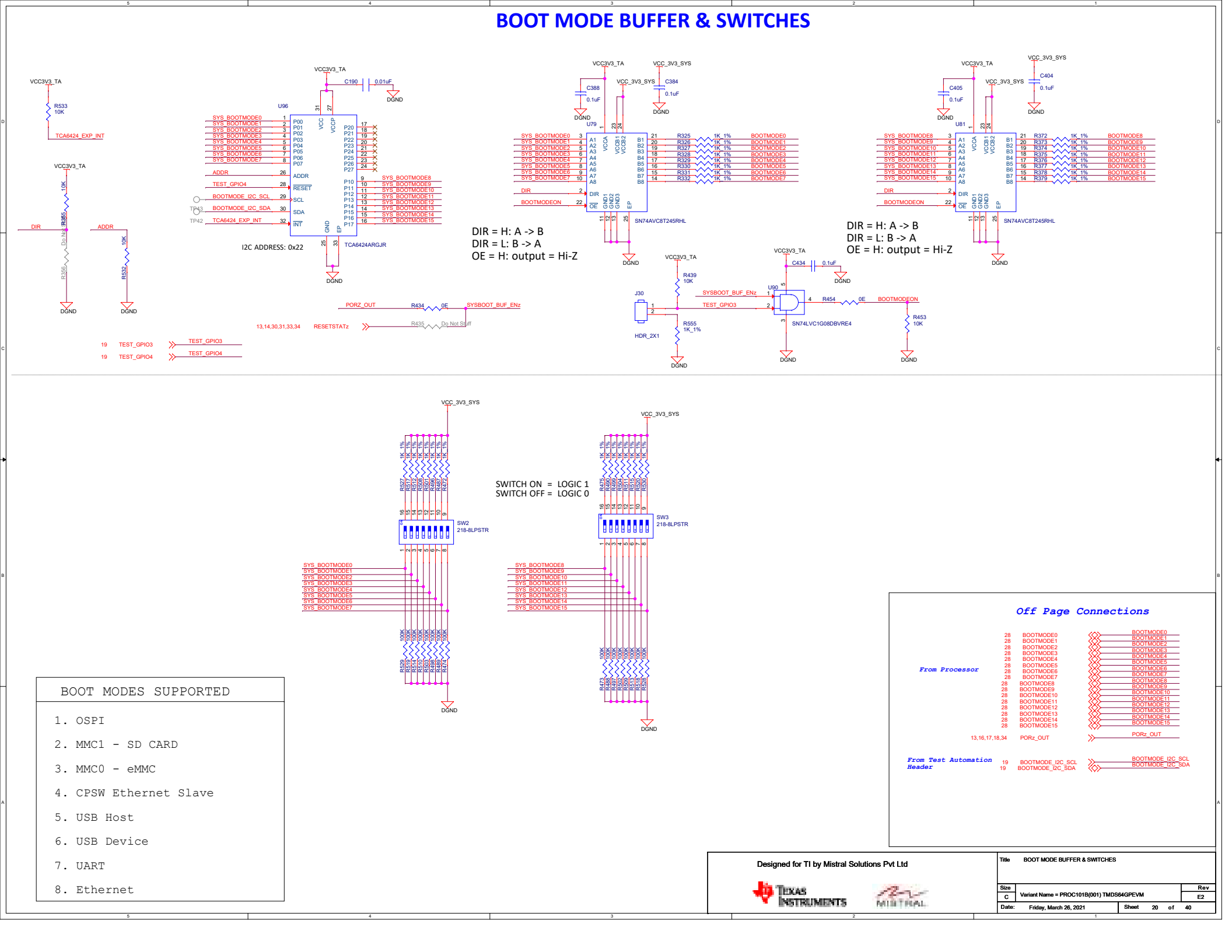
1. OSPI
2. MMC1 - SD CARD
3. MMC0 - eMMC
4. CPSW Ethernet Slave
5. USB Host
6. USB Device
7. UART
8. Ethernet

Off Page Connections

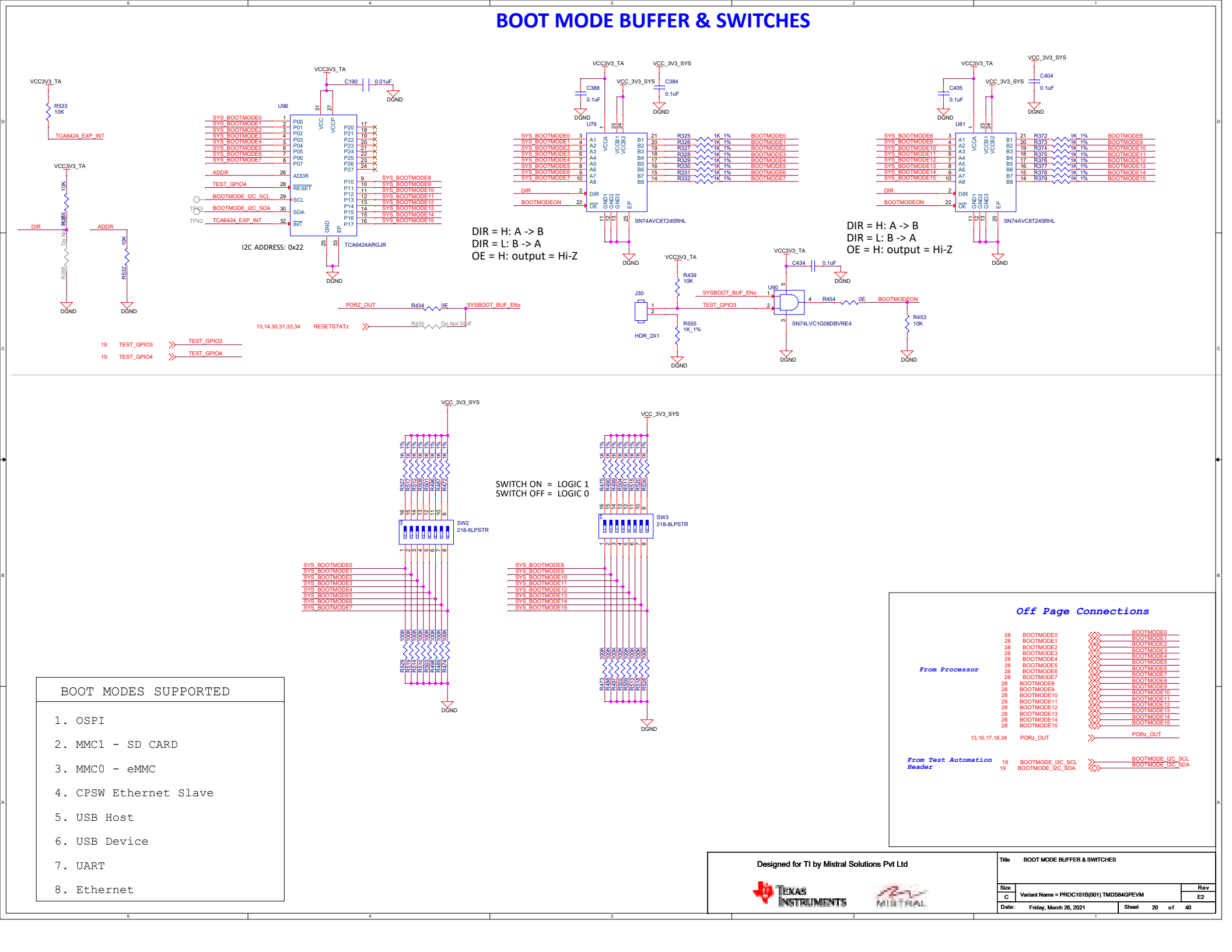
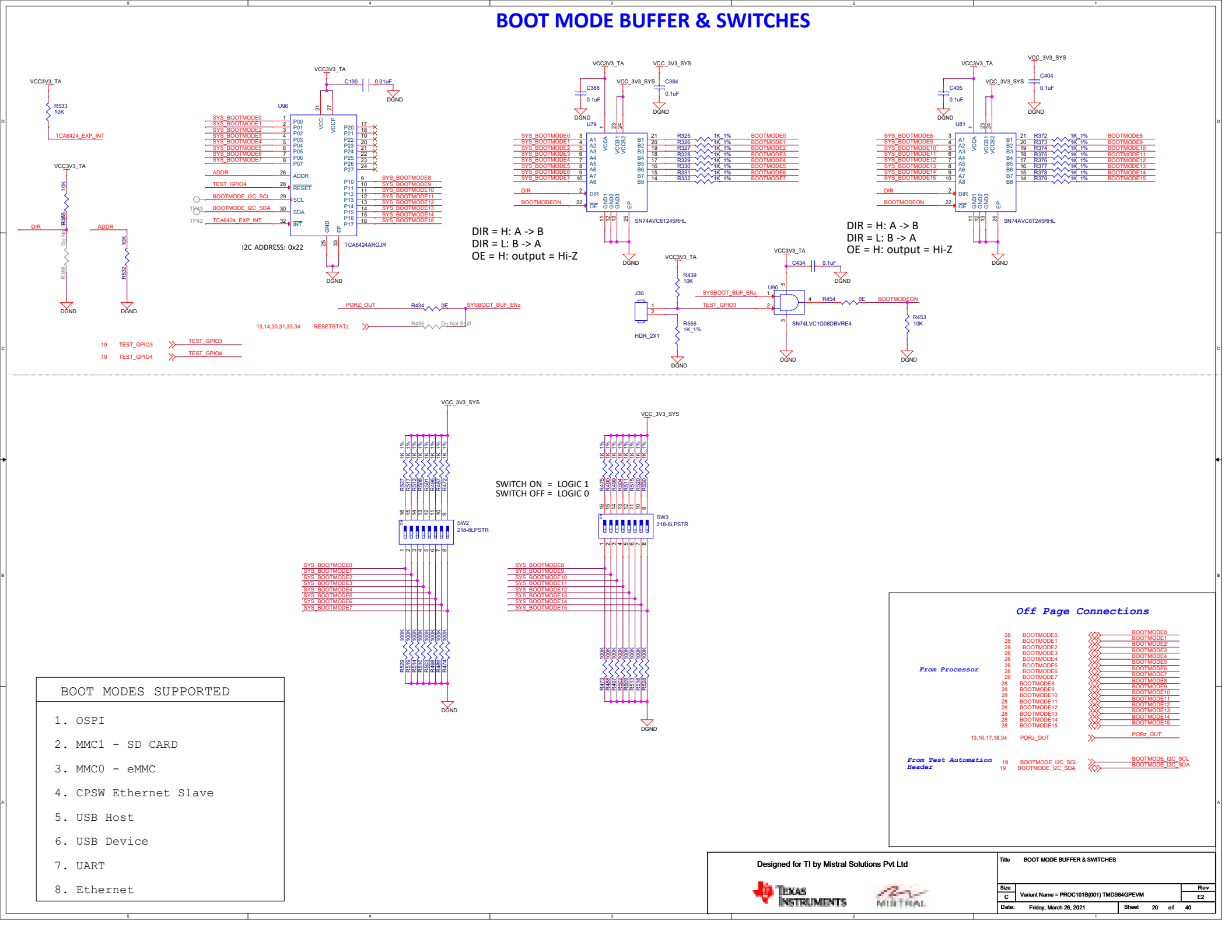
From Processor	<div style="display: flex; justify-content: space-between;"> <div> 28 BOOTMODE0 28 BOOTMODE1 28 BOOTMODE2 28 BOOTMODE3 28 BOOTMODE4 28 BOOTMODE5 28 BOOTMODE6 28 BOOTMODE7 28 BOOTMODE8 28 BOOTMODE9 28 BOOTMODE10 28 BOOTMODE11 28 BOOTMODE12 28 BOOTMODE13 28 BOOTMODE14 28 BOOTMODE15 </div> <div> 28 BOOTMODE0 28 BOOTMODE1 28 BOOTMODE2 28 BOOTMODE3 28 BOOTMODE4 28 BOOTMODE5 28 BOOTMODE6 28 BOOTMODE7 28 BOOTMODE8 28 BOOTMODE9 28 BOOTMODE10 28 BOOTMODE11 28 BOOTMODE12 28 BOOTMODE13 28 BOOTMODE14 28 BOOTMODE15 </div> </div>	<div style="display: flex; justify-content: space-between;"> <div> 13,16,17,18,34 PORz_OUT </div> <div> >>> PORz_OUT </div> </div>
From Test Automation Header	<div style="display: flex; justify-content: space-between;"> <div> 19 BOOTMODE_I2C_SCL 19 BOOTMODE_I2C_SDA </div> <div> >>> BOOTMODE_I2C_SCL >>> BOOTMODE_I2C_SDA </div> </div>	

Designed for TI by Mistral Solutions Pvt Ltd

Title		BOOT MODE BUFFER & SWITCHES	
Size	Variant Name = PROC101B(001) TMSD64GPEVM	Rev	
C		E2	
Date:	Friday, March 26, 2021	Sheet	20 of 40



BOOT MODE BUFFER & SWITCHES



BOOT MODE BUFFER & SWITCHES

19 TEST_GPIO3 >>> TEST_GPIO3
19 TEST_GPIO4 >>> TEST_GPIO4

DIR = H: A -> B
DIR = L: B -> A
OE = H: output = Hi-Z

DIR = H: A -> B
DIR = L: B -> A
OE = H: output = Hi-Z

SW2 216-8LPSTR

SW3 216-8LPSTR

BOOT MODES SUPPORTED

- OSPI
- MMC1 - SD CARD
- MMC0 - eMMC
- CPSW Ethernet Slave
- USB Host
- USB Device
- UART
- Ethernet

Off Page Connections

From Processor	From Test Automation Header
28 BOOTMODE0	19 BOOTMODE_I2C_SCL
28 BOOTMODE1	19 BOOTMODE_I2C_SDA
28 BOOTMODE2	
28 BOOTMODE3	
28 BOOTMODE4	
28 BOOTMODE5	
28 BOOTMODE6	
28 BOOTMODE7	
28 BOOTMODE8	
28 BOOTMODE9	
28 BOOTMODE10	
28 BOOTMODE11	
28 BOOTMODE12	
28 BOOTMODE13	
28 BOOTMODE14	
28 BOOTMODE15	

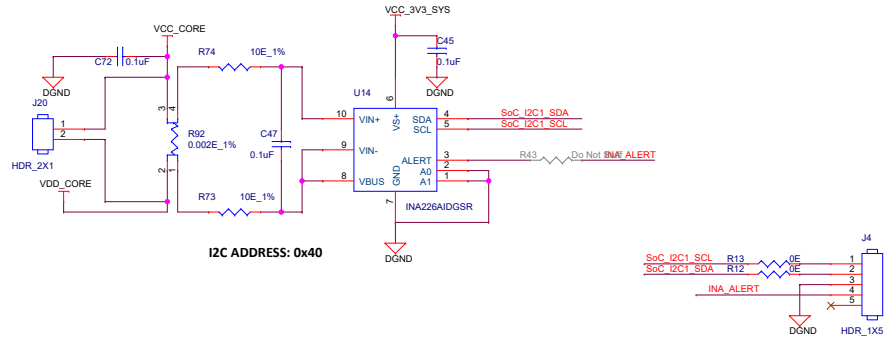
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BOOT MODE BUFFER & SWITCHES

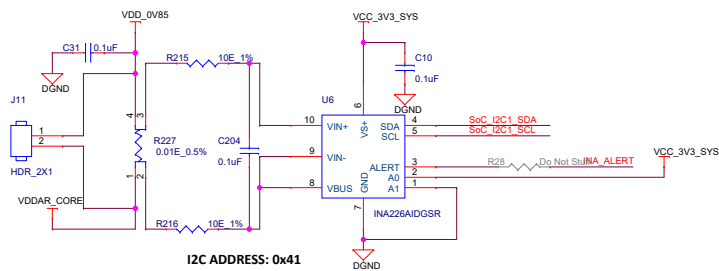
Size	Variant Name = PROC101B(001) TMSD64GPEVM	Rev
C		E2
Date:	Friday, March 26, 2021	Sheet 20 of 40

CURRENT MONITORING DEVICES

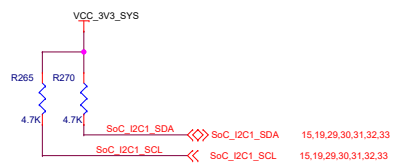
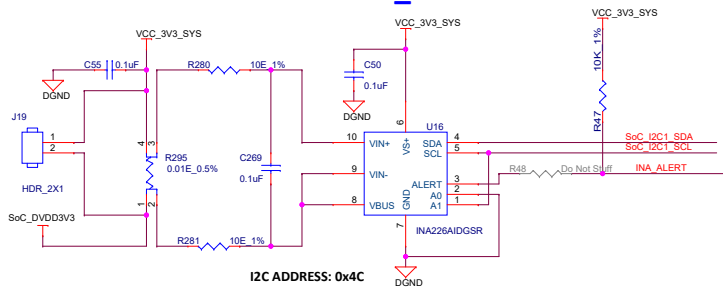
VDD_CORE



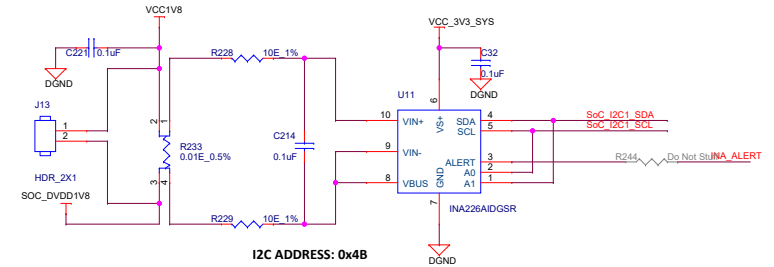
VDDAR_CORE



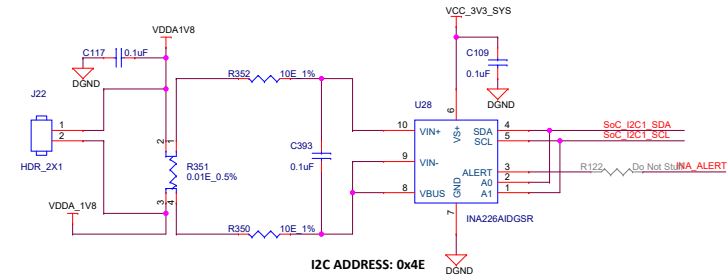
SoC_DVDD3V3



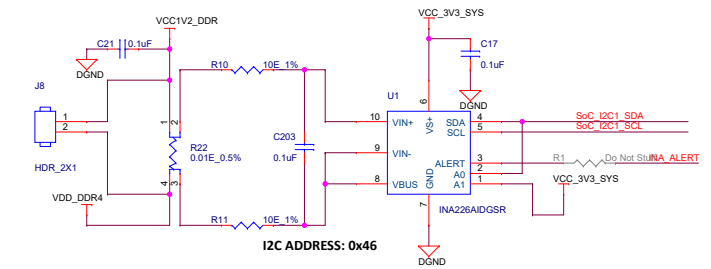
SoC_DVDD1V8



VDDA_1V8



VDD_DDR4



INA I2C SLAVE ADDRESS		
POWER SOURCE	SUPPLY NET	SLAVE ADDRESS (IN HEX)
VCC_CORE	VDD_CORE	40
VDD_0V85	VDDAR_CORE	41
VCC_3V3_SYS	SoC_DVDD3V3	4C
VCC1V8	SoC_DVDD1V8	4B
VDDA1V8	VDDA_1V8	4E
VCC1V2_DDR	VDD_DDR4	46

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Title CURRENT MONITORING DEVICES

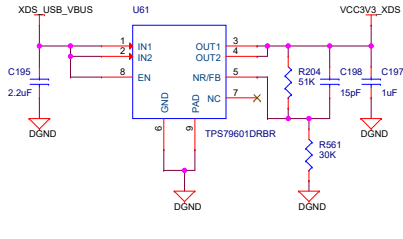
Size Variant Name = PROC101B(001) TMS64GPEVM

Date: Friday, March 26, 2021

Sheet 21 of 40

Rev E2

USB Connector

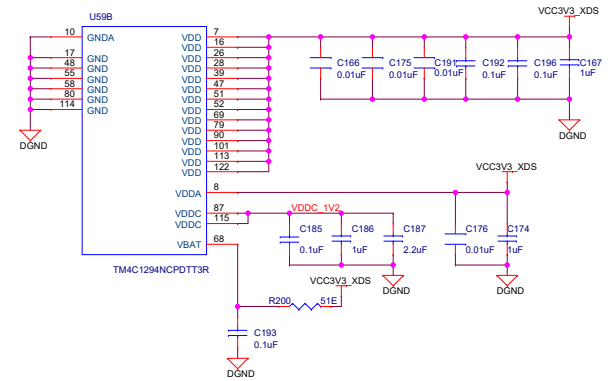


VCC3V3_XDS

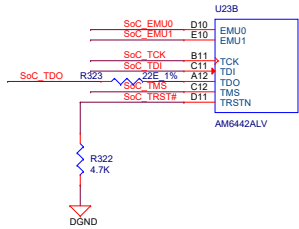
R202
4.7K

R203
4.7K

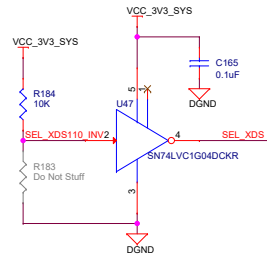
EMU0
EMU1



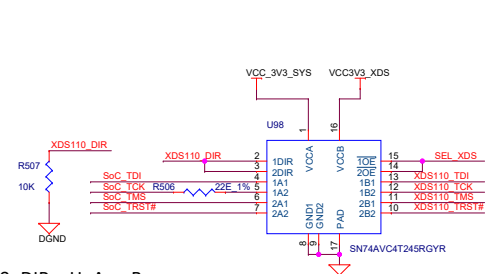
JTAG SoC SECTION



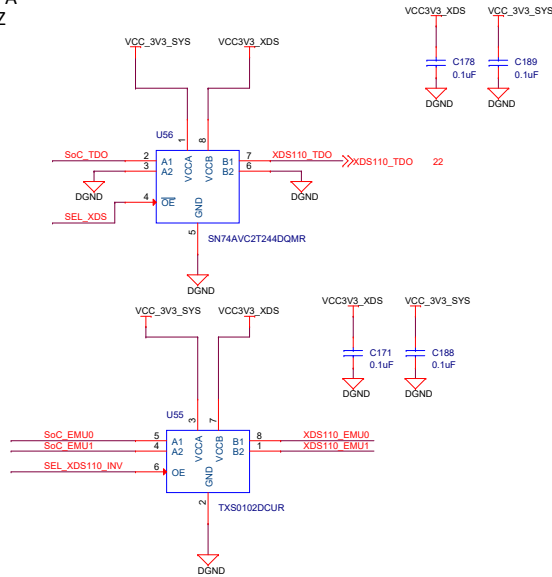
JTAG BUFFER



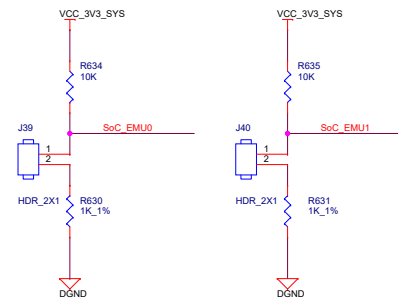
BUFFER XDS110



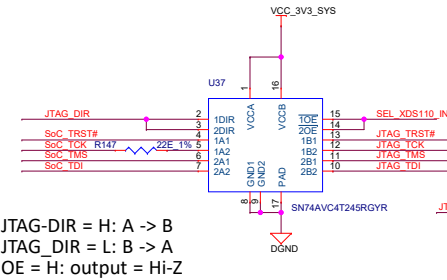
XDS110_DIR = H: A -> B
XDS110_DIR = L: B -> A
OE = H: output = Hi-Z



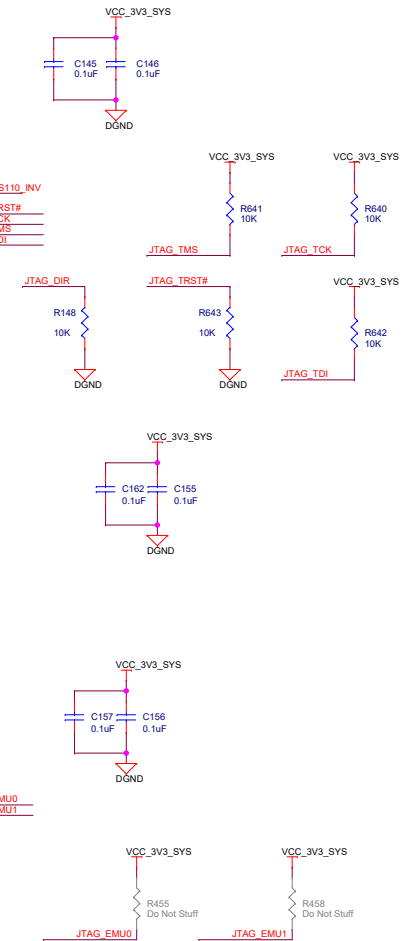
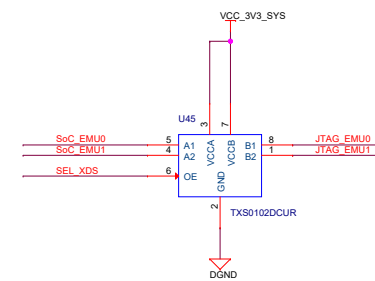
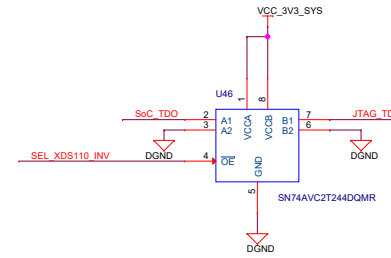
Placement of Buffers U37, U46, U56 and U98 to be changed to reduce Stub length of the JTAG signals. These buffers need to be placed closer to the cTI-20pin connector -J25



BUFFER 20 PIN JTAG



JTAG-DIR = H: A -> B
JTAG-DIR = L: B -> A
OE = H: output = Hi-Z



Off Page Connections

24	SEL_XDS110_INV	SEL_XDS110_INV
24	JTAG_EMU0	JTAG_EMU0
24	JTAG_EMU1	JTAG_EMU1
22	XDS110_TDI	XDS110_TDI
22	XDS110_TCK	XDS110_TCK
22	XDS110_TMS	XDS110_TMS
22	XDS110_TRST#	XDS110_TRST#
24	JTAG_TDI	JTAG_TDI
24	JTAG_TCK	JTAG_TCK
24	JTAG_TMS	JTAG_TMS
24	JTAG_TRST#	JTAG_TRST#
24	JTAG_TDO	JTAG_TDO
22	XDS110_EMU0	XDS110_EMU0
22	XDS110_EMU1	XDS110_EMU1

From XDS1100 Debugger

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Title JTAG BUFFER

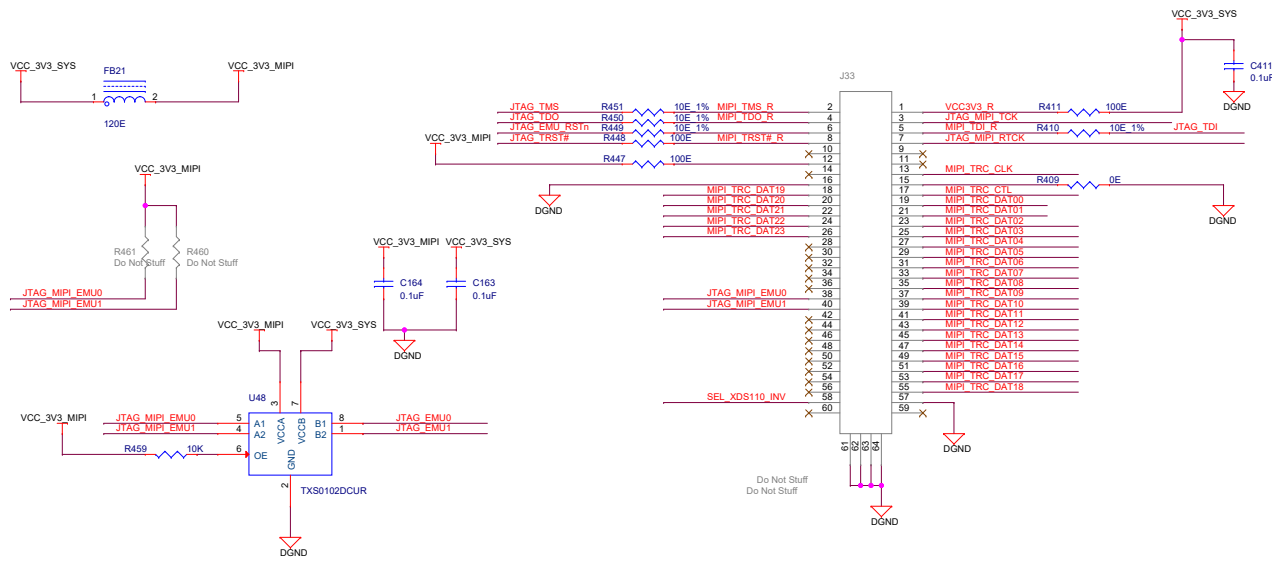
Size Variant Name = PROC101B(001) TMS64GPEVM

Date: Friday, March 26, 2021

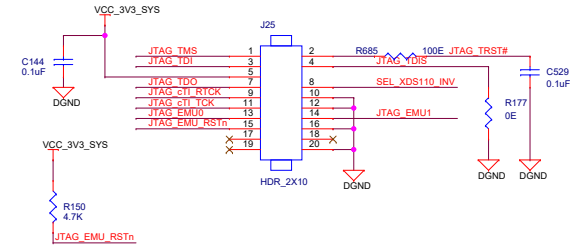
Rev E2

Sheet 23 of 40

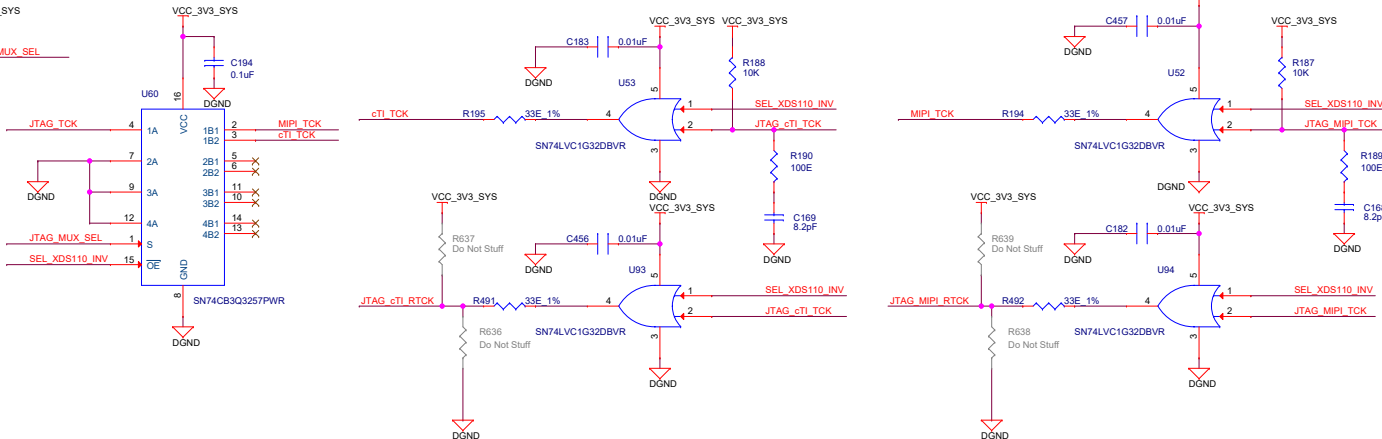
MIPI 60 PIN CONNECTOR



JTAG 20 PIN cTI CONNECTOR



JTAG CLOCK BUFFER

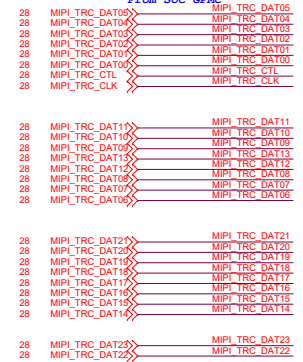


Off Page Connections

From JTAG Buffer



From SoC GPMC



Designed for TI by Mistral Solutions Pvt Ltd



Title: MIPI 60 PIN CONNECTOR

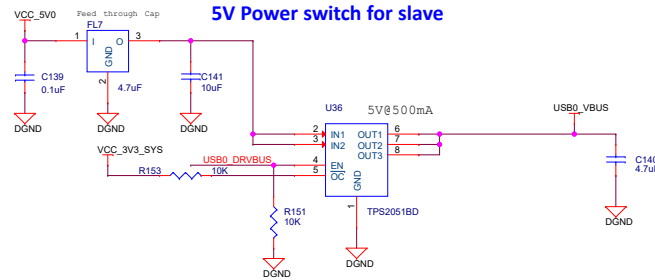
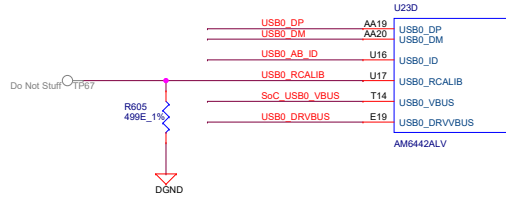
Size: Variant Name = PROC101B(001) TMS64GPEVM

Date: Friday, March 26, 2021

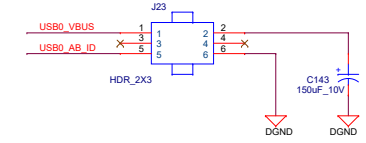
Sheet: 24 of 40

Rev: E2

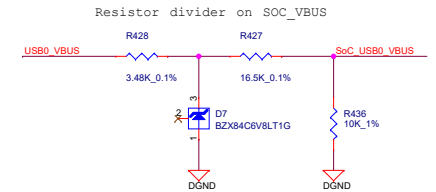
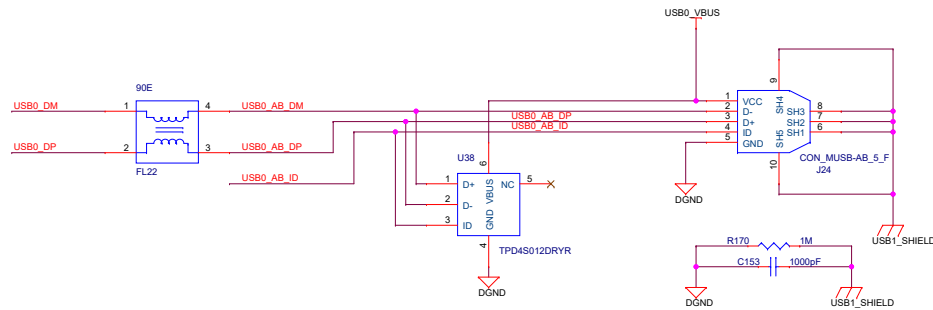
USB 2.0 INTERFACE



2X3 header to enable bulk capacitance on USB0_VBUS in host mode and to ground USB0_AB_ID pin, if a non standard cable is used



Micro USB 2.0 AB Connector



Designed for TI by Mistral Solutions Pvt Ltd



Title			Rev
USB 2.0 INTERFACE			E2
Size	Variant Name = PROC101B(001) TMS64GPEVM		Rev
C			E2
Date:	Friday, March 26, 2021	Sheet	25 of 40

The schematic diagram illustrates the internal circuitry of the FT4232 USB-to-UART bridge module. The central component is the FT4232L IC, which is connected to various power and signal lines. The power supply section includes VCC_1V8_FT4232, VPHY_3V3_FT4232, VPLL_3V3_FT4232, and VCC_3V3_FT4232. The IC is connected to these lines via pins 4, 5, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, 71, 72, 73, 74, 75, 76, 77, 78, 79, 80, 81, 82, 83, 84, 85, 86, 87, 88, 89, 90, 91, 92, 93, 94, 95, 96, 97, 98, 99, 100. The IC is also connected to a USB interface via pins 1-10 and to a UART interface via pins 11-19. The module includes a reset pin (RESET) and a test pin (TEST). The schematic shows the internal components of the module, including the FT4232L IC, various capacitors (C441, C416, C438, C433), resistors (R175, R464), and a crystal (Y3). The module is powered by VCC_1V8_FT4232, VPHY_3V3_FT4232, VPLL_3V3_FT4232, and VCC_3V3_FT4232. It features a USB interface with DM and DP lines, and a UART interface with RX and TX lines. The FT4232L IC is connected to the USB interface via pins 1-10 and to the UART interface via pins 11-19. The module also includes a reset pin (RESET) and a test pin (TEST).

SOC_MAIN_UART0_RX_3V3	SOC_MAIN_UART0_RX_3V3	29
SOC_MAIN_UART0_TX_3V3	SOC_MAIN_UART0_TX_3V3	29
SOC_MAIN_UART0_RTS_3V3	SOC_MAIN_UART0_RTS_3V3	29
SOC_MAIN_UART0_CTS_3V3	SOC_MAIN_UART0_CTS_3V3	29
MCU_UART0_RX_3V3	MCU_UART0_RX_3V3	34
MCU_UART0_TX_3V3	MCU_UART0_TX_3V3	34
MCU_UART0_RTS_3V3	MCU_UART0_RTS_3V3	34
MCU_UART0_CTS_3V3	MCU_UART0_CTS_3V3	34
SOC_MAIN_UART1_RX_3V3	SOC_MAIN_UART1_RX_3V3	29
SOC_MAIN_UART1_TX_3V3	SOC_MAIN_UART1_TX_3V3	29
SOC_MAIN_UART1_RTS_3V3	SOC_MAIN_UART1_RTS_3V3	29
SOC_MAIN_UART1_CTS_3V3	SOC_MAIN_UART1_CTS_3V3	29



TEXAS
INSTRUMENTS



Size	
------	--

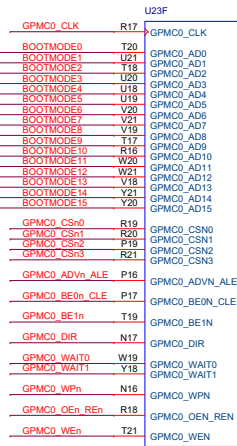
Size	
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C	Variant Name = PROC101B(001) TMDS64GPEVM
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Date: Thursday, October 28, 2021	Sheet
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GPMC

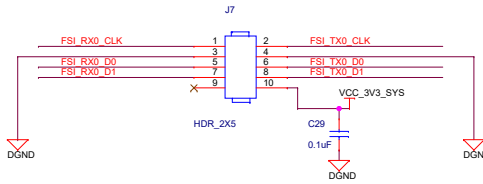
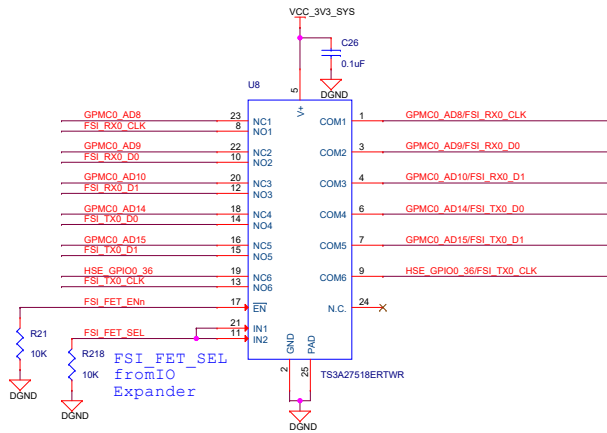
To Boot Mode Buffer ,
HSE & MIPI Conn



AM6442ALV

GPMC TO FSI & HSE CONNECTOR

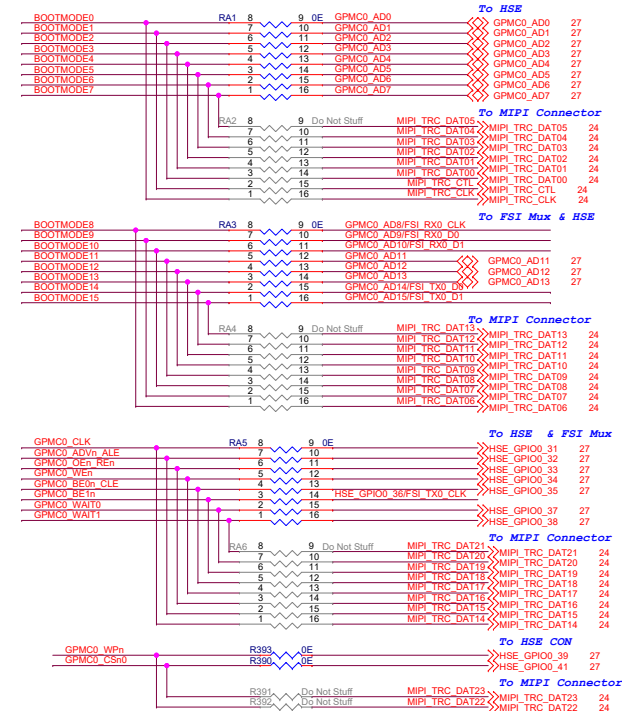
FSI CONNECTOR



TS3A27518ERTWR Truth Table

EN#	IN1	IN2	NC1/2/3 TO COM1/2/3 & COM1/2/3 TO NC1/2/3	NC4/5/6 TO COM1/2/3 & COM1/2/3 TO NC4/5/6	NO1/2/3 TO COM1/2/3 & COM1/2/3 TO NO1/2/3	NO4/5/6 TO COM1/2/3 & COM1/2/3 TO NO4/5/6
H	X	X	OFF	OFF	OFF	OFF
L	L	L	ON	ON	OFF	OFF
L	H	L	OFF	ON	ON	OFF
L	L	H	ON	OFF	OFF	ON
L	H	H	OFF	OFF	ON	ON

0- Ohm Res MUX between HSE Connector and TRACE Functionality
-For HSE Connector RA1, RA3, RA5, R393 & R390 Should be installed and RA2, RA4, RA6, R391& R392 Should be DNI'd.
-For TRACE RA2, RA4, RA6, R391& R392 Should be installed and RA1, RA3, RA5, R393 & R390 Should be DNI'd.



Off Page Connections

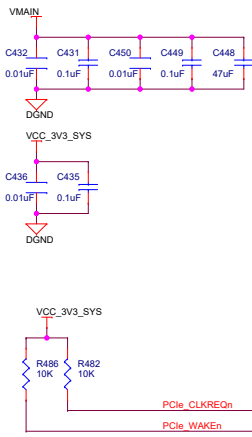
From IO Expander	33	FSI_FET_SEL	FSI_FET_SEL
To HSE Connector	27	GPMC0_CS[0:3]	GPMC0_CS[0:3]
	27	GPMC0_DIR	GPMC0_DIR
From FSI mux	27	GPMC0_AD[0:15]	GPMC0_AD[0:15]
To HSE Connector	27	HSE_GPIO[0:36]	HSE_GPIO[0:36]

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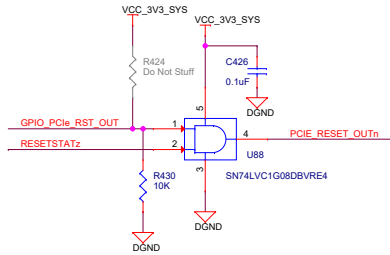


Title	GPMC
Size	Variant Name = PROC101B(001) TMD564GPEVM
C	Date: Friday, March 26, 2021
Rev	E2
Sheet	28 of 40

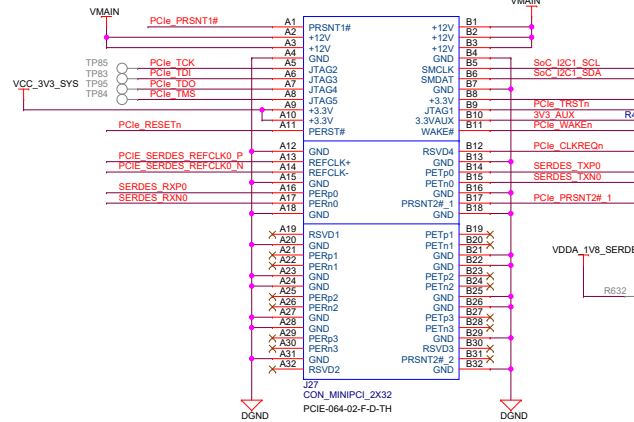
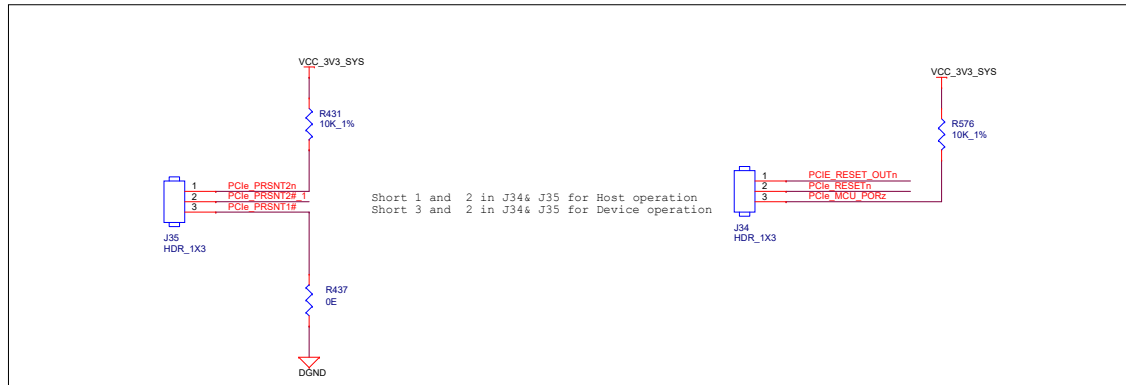
x4 Lane PCIe Connector



PCIe Reset

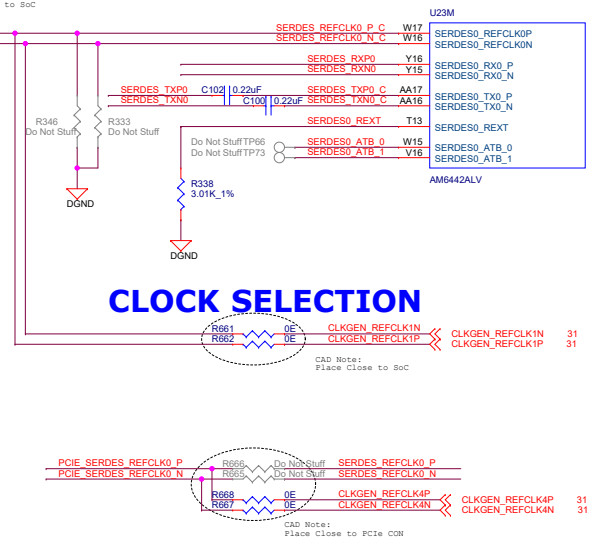


RC OR EP MODE SELECTION



Note:
R679, R680 Mounted with 0E Resistor when PCIe REFCLK is in no Re-biasing Mode.
R679, R680 to be replaced with 100nf CAP 0402 package when PCIe REFCLK is in Re-biasing Mode.

CLOCK SELECTION



Off Page Connections

PCIe MCU PORz	PCIe MCU PORz	34
GPIO PCIe_RST_OUT	GPIO PCIe_RST_OUT	33
RESESTATz	RESESTATz	13,14,20,31,33,34
SoC I2C1_SCL	SoC I2C1_SCL	15,19,21,29,31,32,33
SoC I2C1_SDA	SoC I2C1_SDA	15,19,21,29,31,32,33

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Title

PCIe INTERFACE

Size

PROC101B(001) TMS864GPEVM

Rev

E2

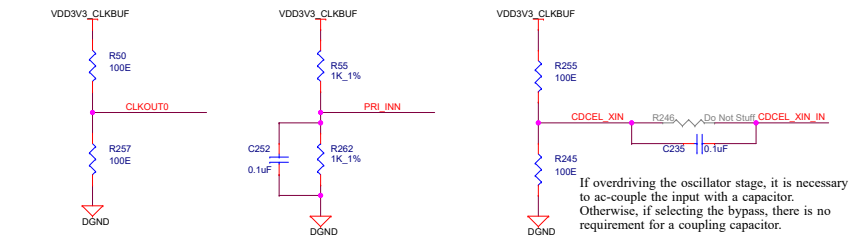
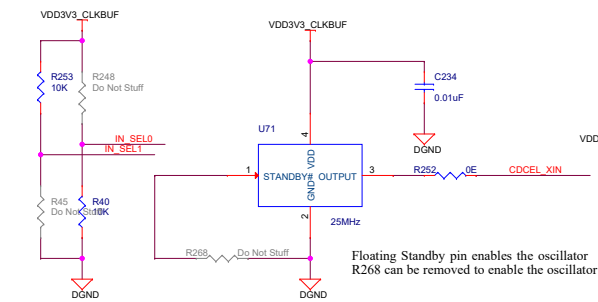
Date:

Friday, March 28, 2021

Sheet

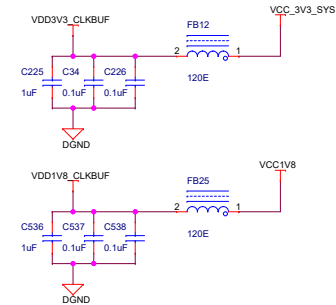
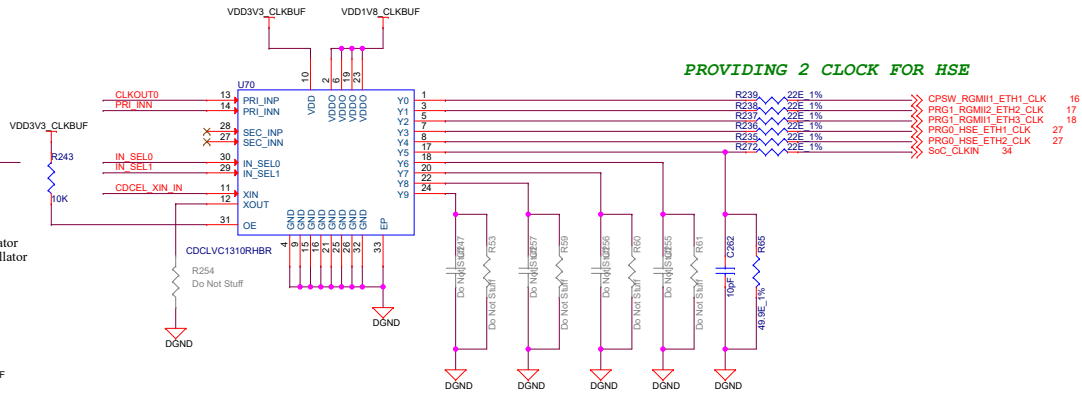
30 of 40

REFERENCE INPUT SELECTION



If overriding the oscillator stage, it is necessary to ac-couple the input with a capacitor. Otherwise, if selecting the bypass, there is no requirement for a coupling capacitor.

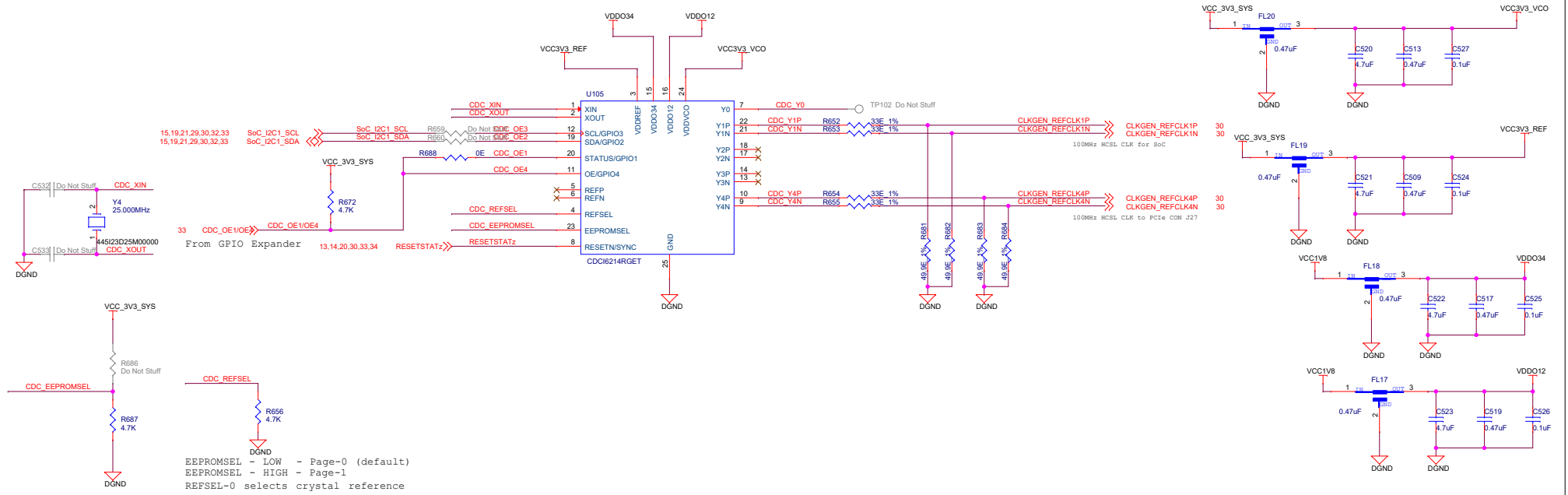
ETHERNET PHY CLOCK BUFFER



Off Page Connections

From SoC CLKOUT0 <--> CLKOUT0 29

PCIe Clock HCSL (100MHz)



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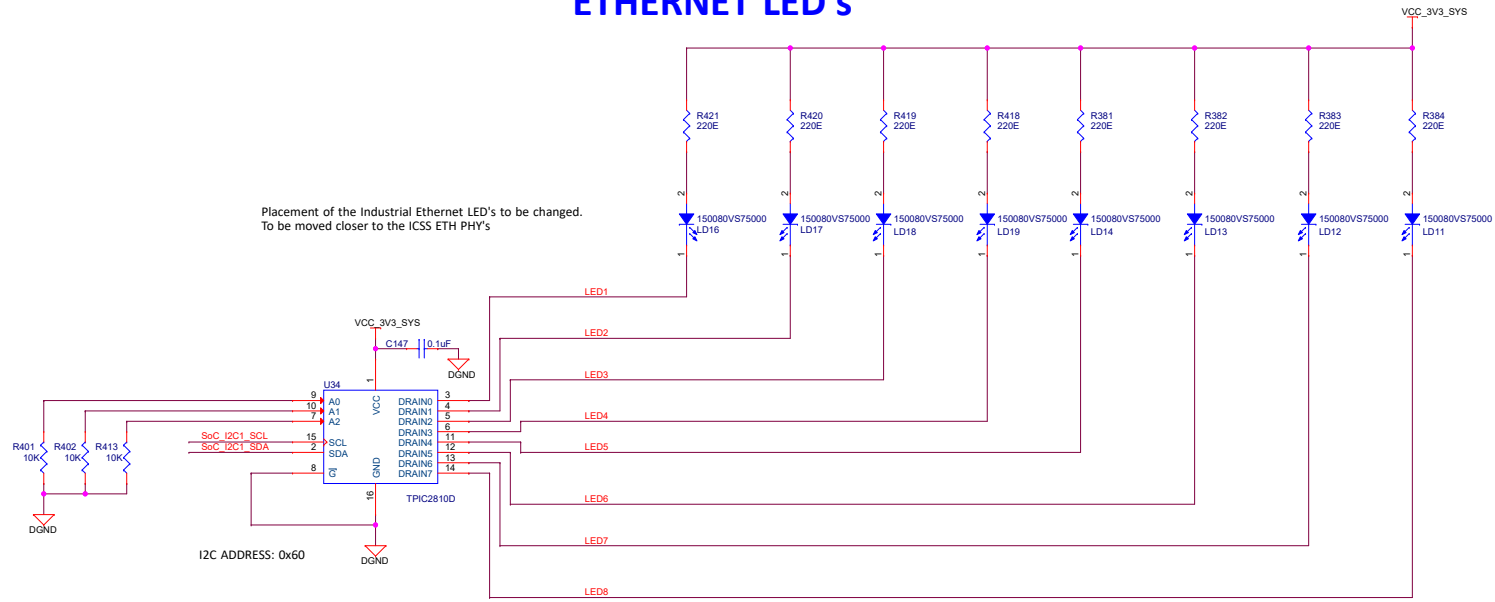


Title ETHERNET PHY & PCIe CLOCK GENERATOR

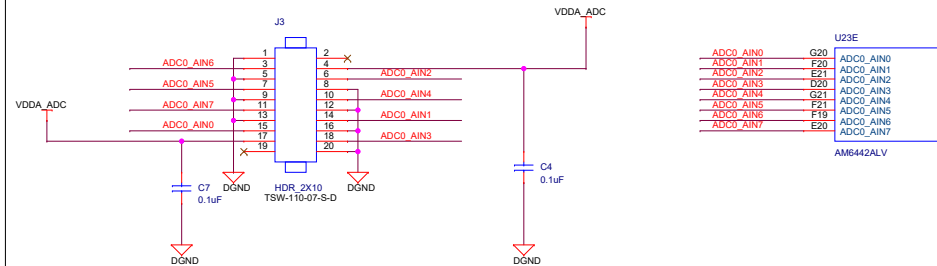
Size	Variant Name = PROC101B(001) TMD864GPEVM	Rev
C		E2

Date: Wednesday, June 09, 2021 Sheet 31 of 40

ETHERNET LED's



ADC CONNECTOR



Off Page Connections

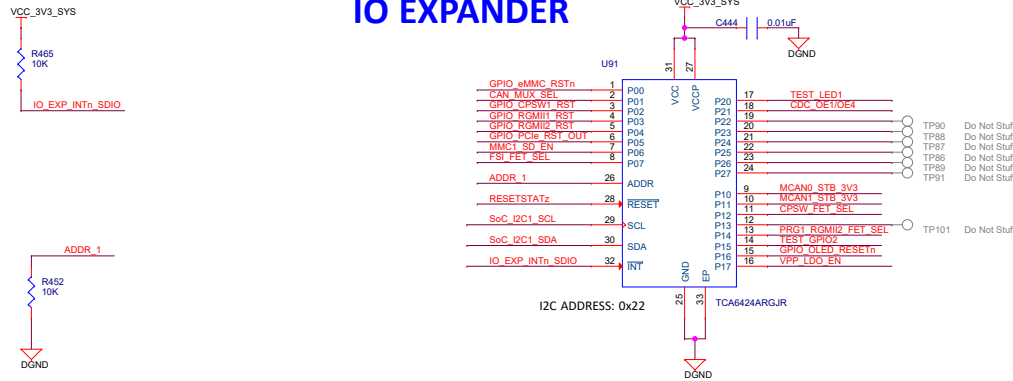
SoC_I2C1_SCL	15, 19, 21, 29, 30, 31, 33
SoC_I2C1_SDA	15, 19, 21, 29, 30, 31, 33

Designed for TI by Mistral Solutions Pvt Ltd

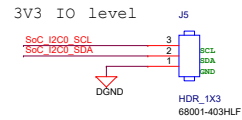


Title		ETHERNET LED's	
Size	Variant Name = PROC101B(001) TMD564GPEVM	Rev	
C		E2	
Date:	Friday, March 26, 2021	Sheet	32 of 40

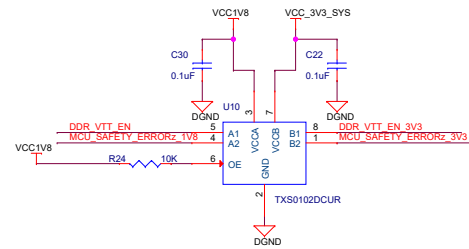
IO EXPANDER



I2C TEST HEADER



LEVEL TRANSLATOR



Off Page Connections

GPIO eMMC_RSTn	GPIO eMMC_RSTn	13	30
GPIO_PCIE_RST_OUT	GPIO_PCIE_RST_OUT	16	30
GPIO_CPSWT1_RST	GPIO_CPSWT1_RST	16	30
GPIO_RGMII1_RST	GPIO_RGMII1_RST	16	30
GPIO_PCIE_RST_OUT	GPIO_PCIE_RST_OUT	16	30
MMC1_SD_EN	MMC1_SD_EN	13	30
FSI_FET_SEL	FSI_FET_SEL	28	30
MCAN0_STB_3V3	MCAN0_STB_3V3	29	30
MCAN1_STB_3V3	MCAN1_STB_3V3	29	30
CPSW_FET_SEL	CPSW_FET_SEL	16	30
PRG1_RGMII2_FET_SEL	PRG1_RGMII2_FET_SEL	17	30
TEST_GPIO2	TEST_GPIO2	19	30
GPIO_OLED_RESETh	GPIO_OLED_RESETh	29	30
VPP_LDO_EN	VPP_LDO_EN	38	30
CAN_MUX_SEL	CAN_MUX_SEL	29	30
TEST_LED1	TEST_LED1	14	30
CDC_OE1OE4	CDC_OE1OE4	31	30
RESETSTATz	RESETSTATz	13,14,20,30,31,32	30
SoC_I2C1_SDA	SoC_I2C1_SDA	15,19,21,29,30,31,32	30
SoC_I2C1_SCL	SoC_I2C1_SCL	15,19,21,29,30,31,32	30
SoC_I2C0_SDA	SoC_I2C0_SDA	15,27,29	30
SoC_I2C0_SCL	SoC_I2C0_SCL	15,27,29	30

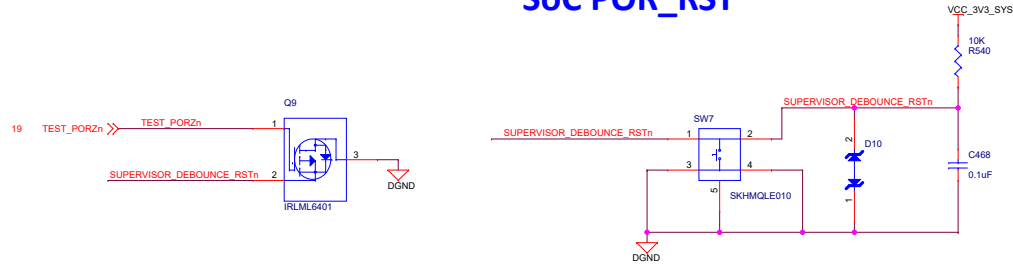
From Safety Connector	MCU SAFETY_ERRORz_3V3	34
From SoC OSPI Section	DDR_VTT_EN	14
To Processor	MCU SAFETY_ERRORz_1V8	34
To VTT Reg	DDR_VTT_EN_3V3	39
To SoC MMC	IO_EXP_INTn_SDIO	13

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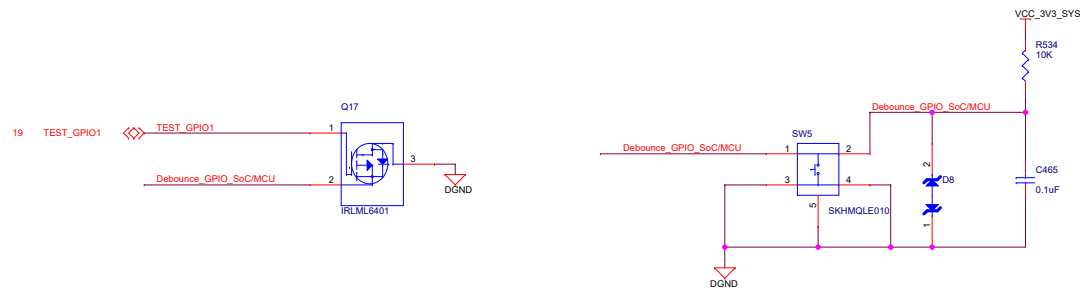
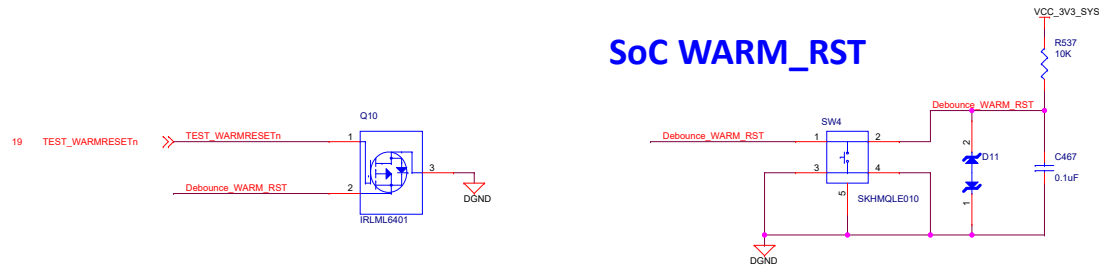


Title IO EXPANDER		
Size	Variant Name = PROC101B(001) TMSD64GPEVM	Rev
C		E2
Date:	Friday, March 26, 2021	Sheet 33 of 40

SoC POR_RST

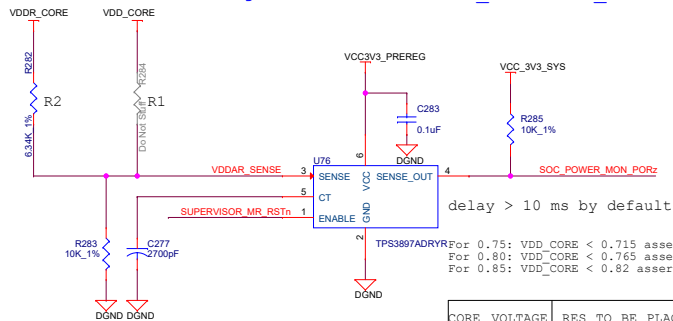


SoC WARM_RST



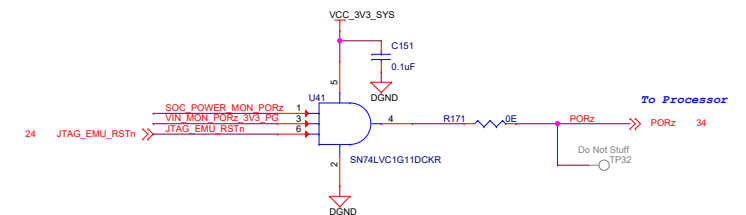
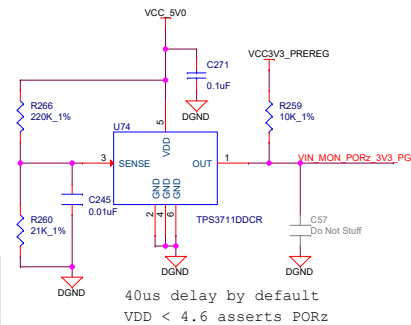
VOLTAGE SUPERVISOR

Core Voltage Monitor (VDDAR_CORE/VDD_CORE)

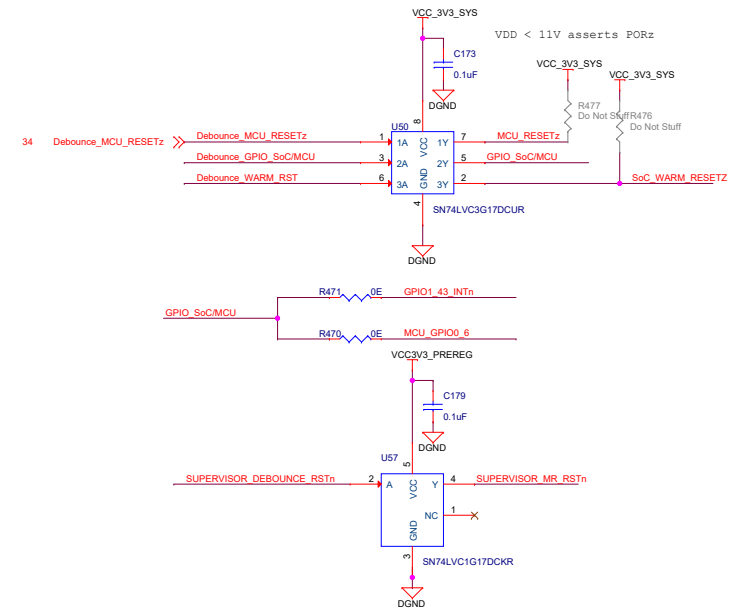


CORE VOLTAGE	RES TO BE PLACED
0.75V	R1 = 4.3K
0.80V	R2 = 5.23K
0.85V	R2 = 6.34K

5V OUTPUT MONITOR (VCC_5V0)



DEBOUNCE CIRCUIT



Off Page Connections

To Processor	VIN_MON_PORz_3V3_PG	VIN_MON_PORz_3V3_PG	37,39
	SoC_WARM_RESETz	SoC_WARM_RESETz	34
	GPIO1_43_INTn	GPIO1_43_INTn	29
	MCU_RESETz	MCU_RESETz	27,34
	MCU_GPIO_6	MCU_GPIO_6	34

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Title DEBOUNCE CIRCUIT & VOLTAGE SUPERVISOR

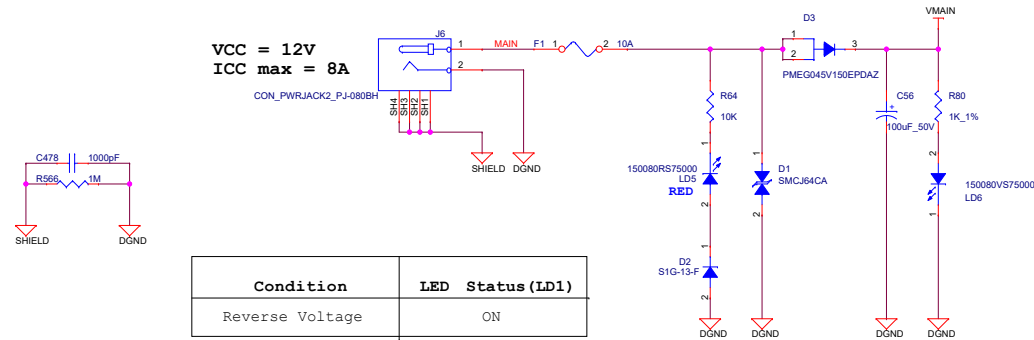
Size Variant Name = PROC101B(001) TMS64GPEVM

Date: Tuesday, March 30, 2021

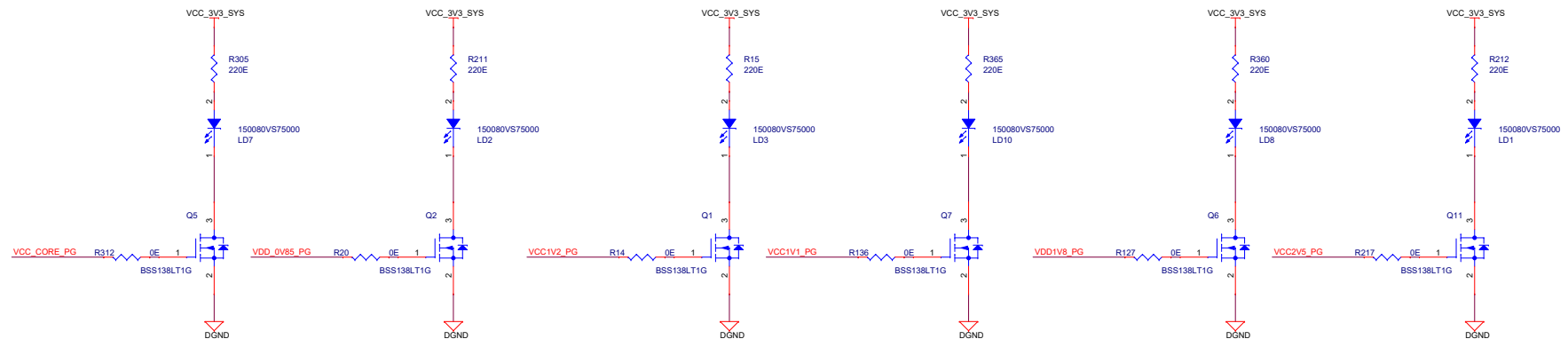
Rev E2

Sheet 35 of 40

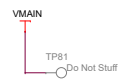
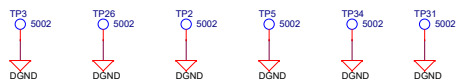
MAIN INPUT 12V DC



POWER INDICATION LED'S



Ground test points



Off Page Connections

VCC_CORE_PG	VCC_CORE_PG	37,38
VDD_0V85_PG	VDD_0V85_PG	38
VCC1V2_PG	VCC1V2_PG	38
VCC1V1_PG	VCC1V1_PG	39
VDD1V8_PG	VDD1V8_PG	38
VCC2V5_PG	VCC2V5_PG	39

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Title MAIN 12V POWERSUPPLY

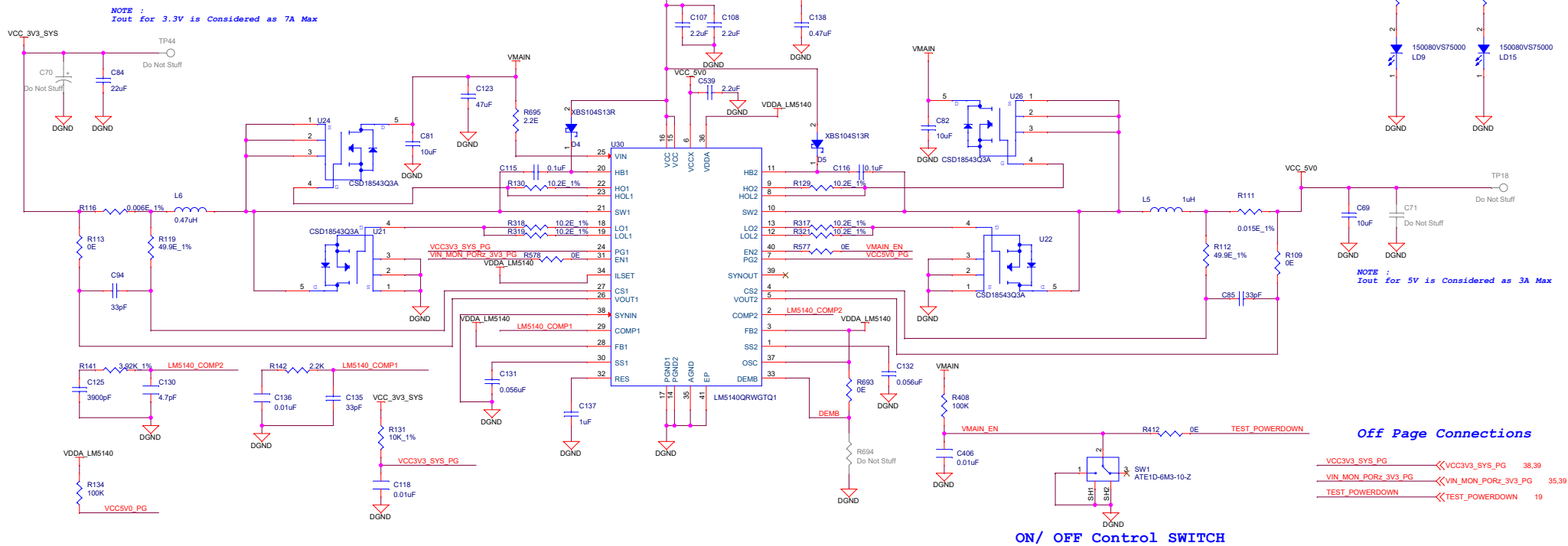
Size Variant Name = PROC101B(001) TMD564GPEVM

Rev E2

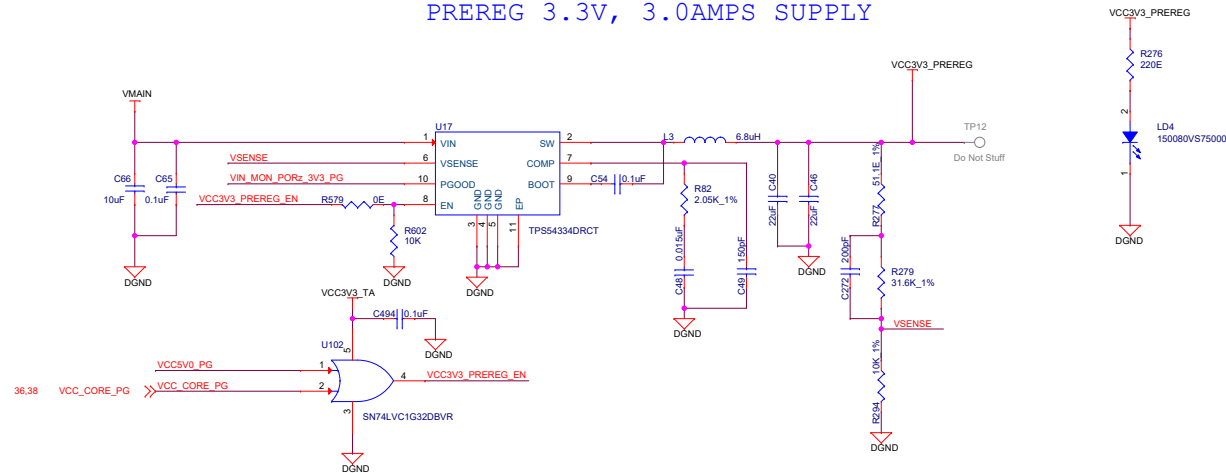
Date: Wednesday, December 01, 2021 Sheet 36 of 40

VCC3V3_SYS & VCC_5V0 POWER SUPPLY

5V, 3A and 3.3V, 7A Dual SUPPLY



PREREG 3.3V, 3.0AMPS SUPPLY



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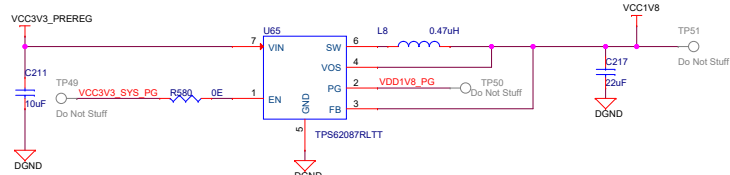
Title DUAL & PREREG REGULATOR

Size Variant Name = PROC101B(001) TMS64GPEVM

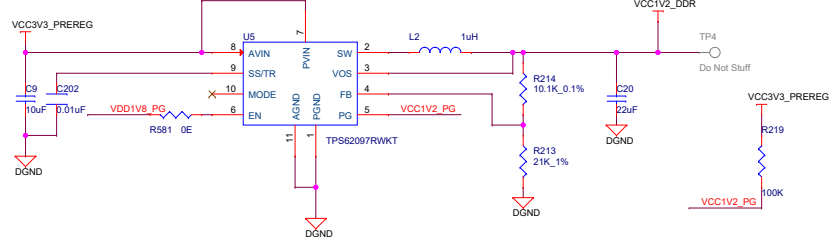
Date: Thursday, December 02, 2021 Sheet 37 of 40

SoC POWER SUPPLY

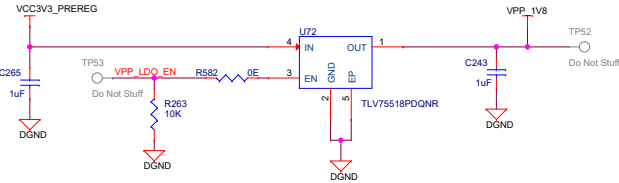
1.8V IO, 3.0AMPS SUPPLY



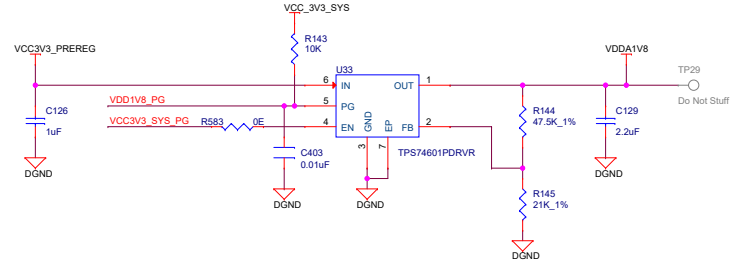
1.2V, 2.0AMPS SUPPLY



1.8V VPP, 0.15AMPS SUPPLY



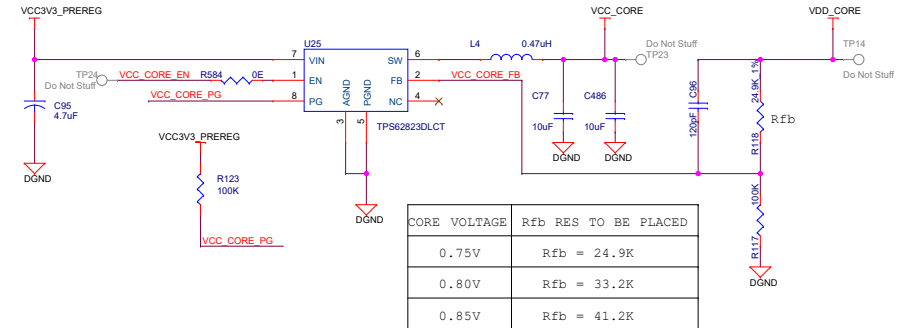
1.8V Analog , 1AMPS SUPPLY



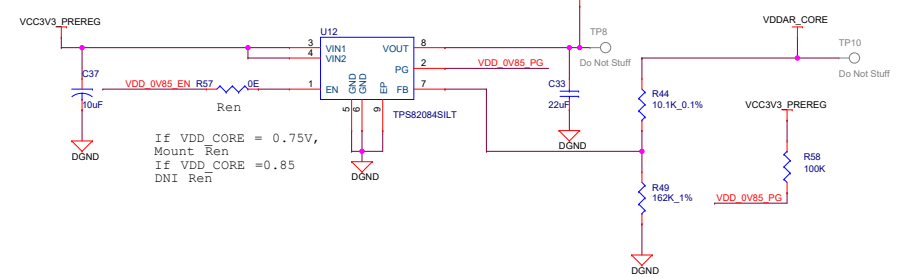
Off Page Connections

36,37	VCC_CORE_PG	VCC_CORE_PG
36	VDD_0V85_PG	VDD_0V85_PG
36	VCC1V2_PG	VCC1V2_PG
36	VDD1V8_PG	VDD1V8_PG
36	VPP_LDO_EN	VPP_LDO_EN
35,37,39	VIN_MON_POR2_3V3_PG	VIN_MON_POR2_3V3_PG
37,39	VCC3V3_SYS_PG	VCC3V3_SYS_PG

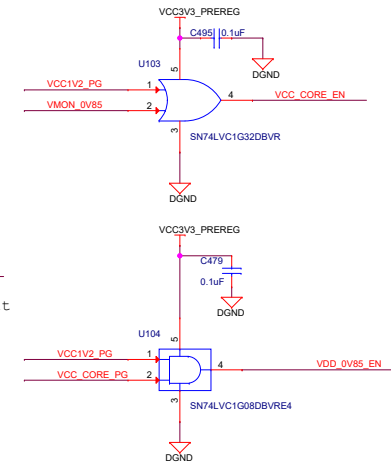
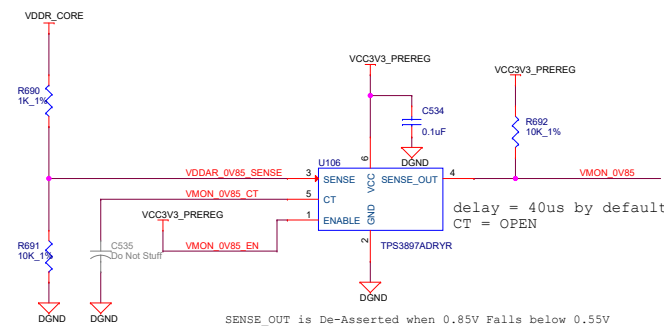
0.75 / 0.8 / 0.85V, 3.0AMPS SUPPLY



0.85 V, 1.5AMPS SUPPLY



0.85V Voltage Monitor for Power Down Sequence



Designed for TI by Mistral Solutions Pvt Ltd



Title SoC POWER SUPPLY

Size Variant Name = PROC101B(001) TMD564GPEVM

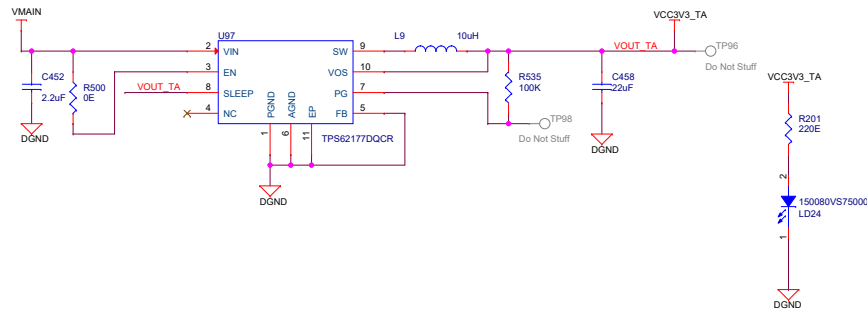
Date: Monday, May 10, 2021

Sheet 38 of 40

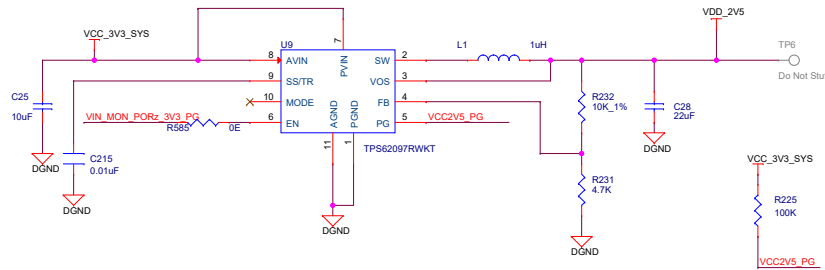
Rev E2

PERIPHERAL POWER SUPPLY

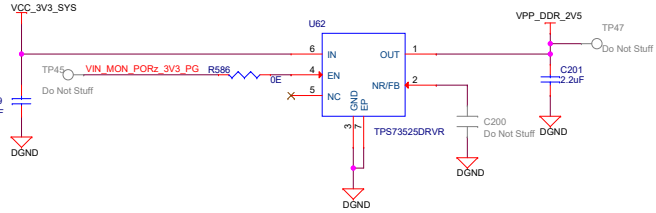
TEST AUTOMATION BOARD POWER



2.5V, 2.0AMPS SUPPLY



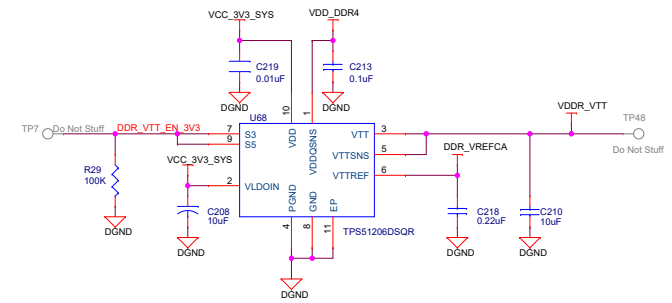
2.5V, .5 AMPS SUPPLY



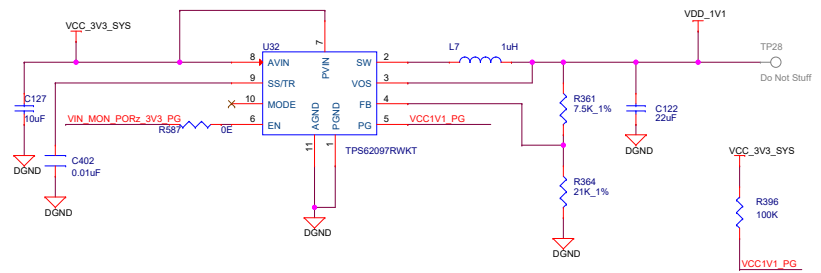
Off Page Connections

33	DDR_VTT_EN_3V3	DDR_VTT_EN_3V3
36	VCC2V5_PG	VCC2V5_PG
36	VCC1V1_PG	VCC1V1_PG
37,38	VCC3V3_SYS_PG	VCC3V3_SYS_PG
35,37	VIN_MON_PORz_3V3_PG	VIN_MON_PORz_3V3_PG

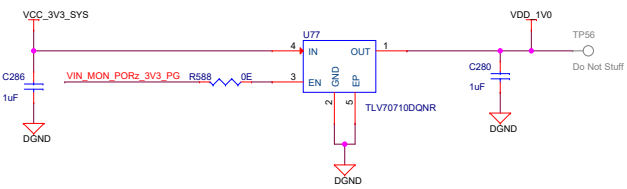
VTT SUPPLY FOR DDR4



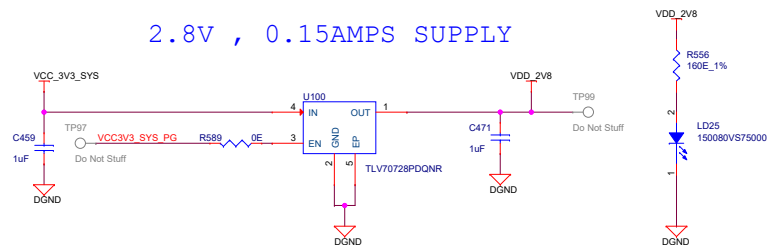
1.1V ETHERNET PHY POWER SUPPLY



1.0V ETHERNET PHY POWER SUPPLY



2.8V , 0.15AMPS SUPPLY



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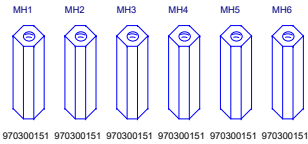
Title			PERIPHERAL POWER SUPPLY
Size	Variant Name = PROC101B(001) TMS64GPEVM	Rev	
C		E2	
Date:	Friday, March 26, 2021	Sheet	39 of 40

HARDWARE SCHEMATICS

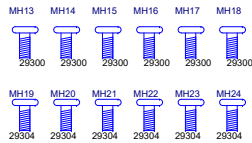
ASSEMBLY NOTES

- 1. All MSL components should be baked as per JEDEC standard.
- 2. PCB should be baked at 120 degree for 8 hours.
- 3. Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified.
- 4. These assemblies are ESD sensitive, ESD precautions shall be observed.
- 5. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
- 6. Provide serial numbers to the assembled boards for identification.
- 7. The assembled board are wrapped in ESD Covers(individual) and packed securely before shipment.

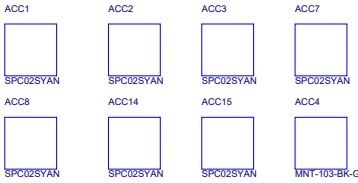
STANDOFFS



SCREWS



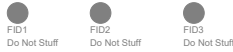
JUMPERS



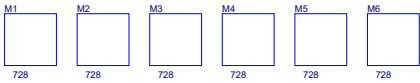
WASHER'S



FIDUCIALS



RUBBER FEET



TI EVM FLYERS



Socket & Processor as Accessories



BARE PCB



LABELS

ORDERABLE PART NO

Board Serial No.



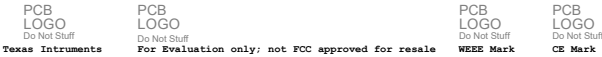
Assembly Revision



Orderable part number

Variant	Label Text
001	TMDS64GPEVM
002	TMDS243GPEVM
003	
004	

LOGOs



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Title HARDWARE SCHEMATICS

Size	Variant Name = PROC101B(001) TMDS64GPEVM	Rev
C		E2
Date:	Friday, March 26, 2021	Sheet 40 of 40